

FIG.1

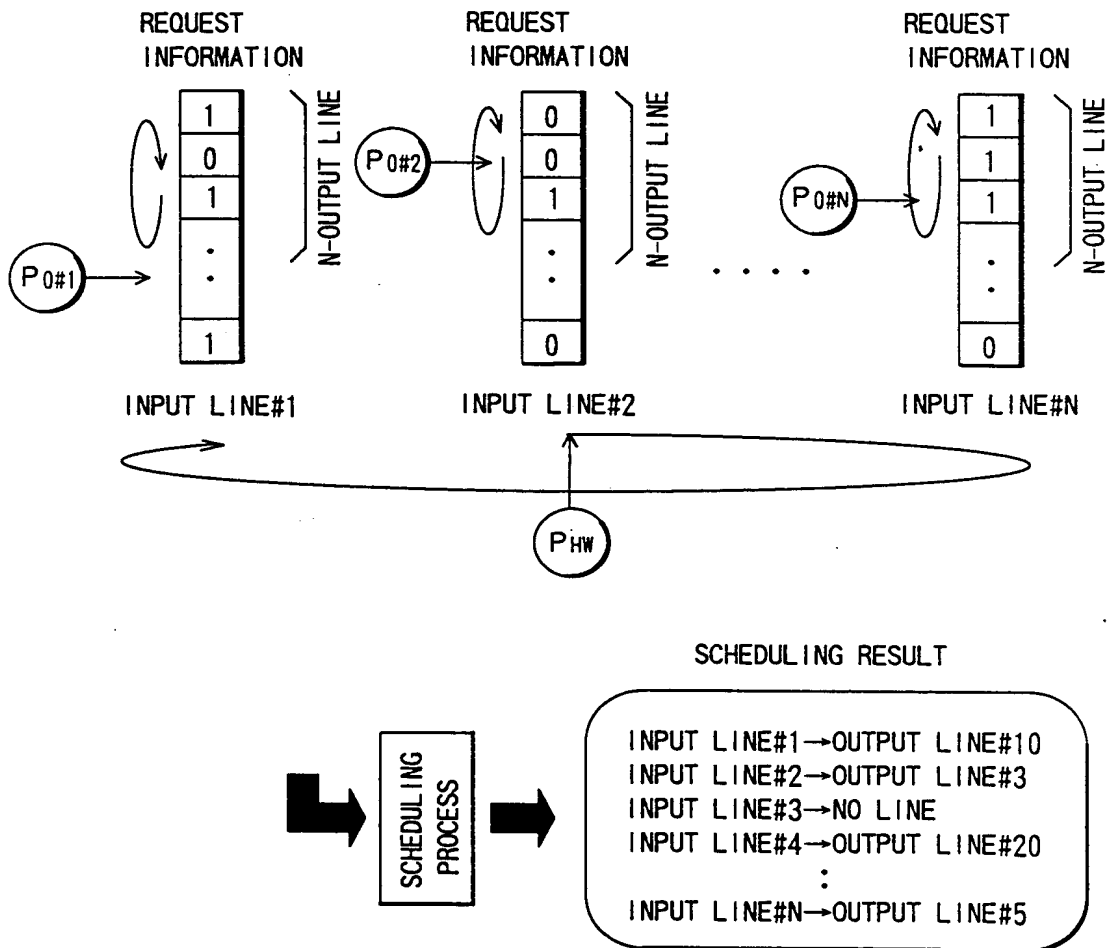
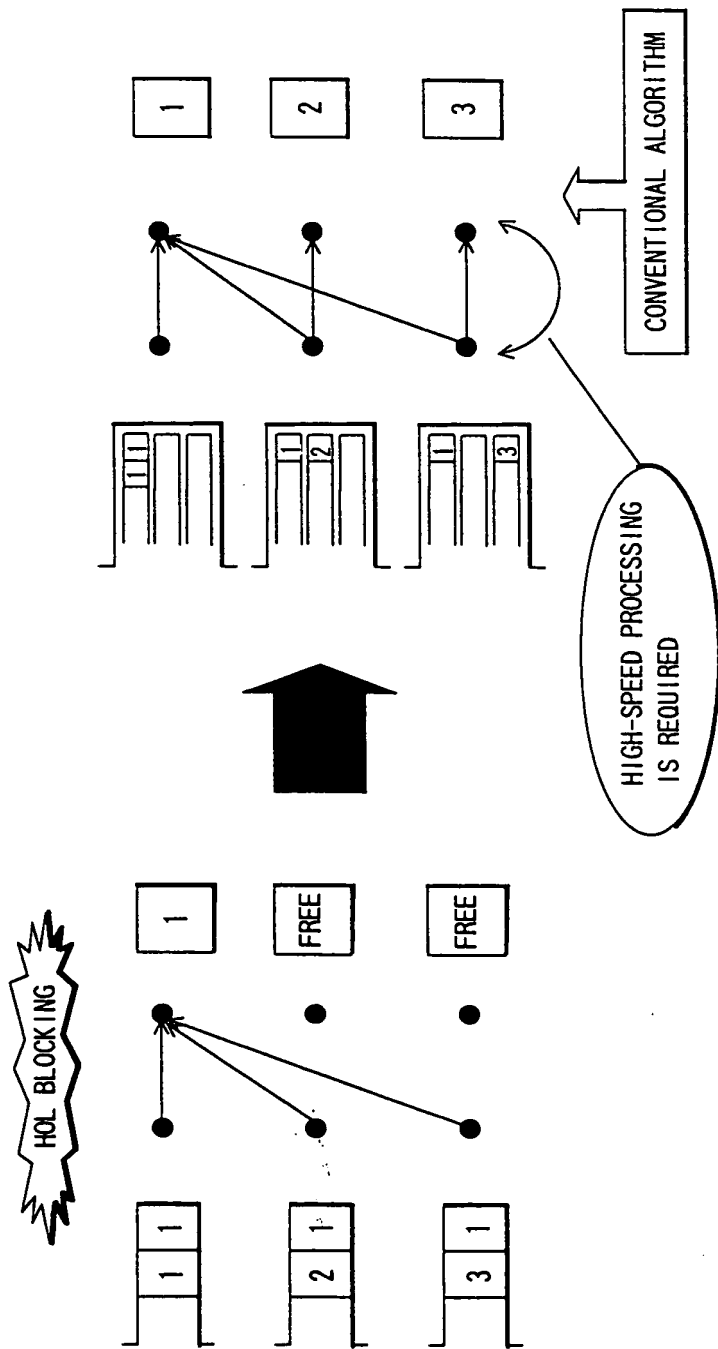


FIG. 2



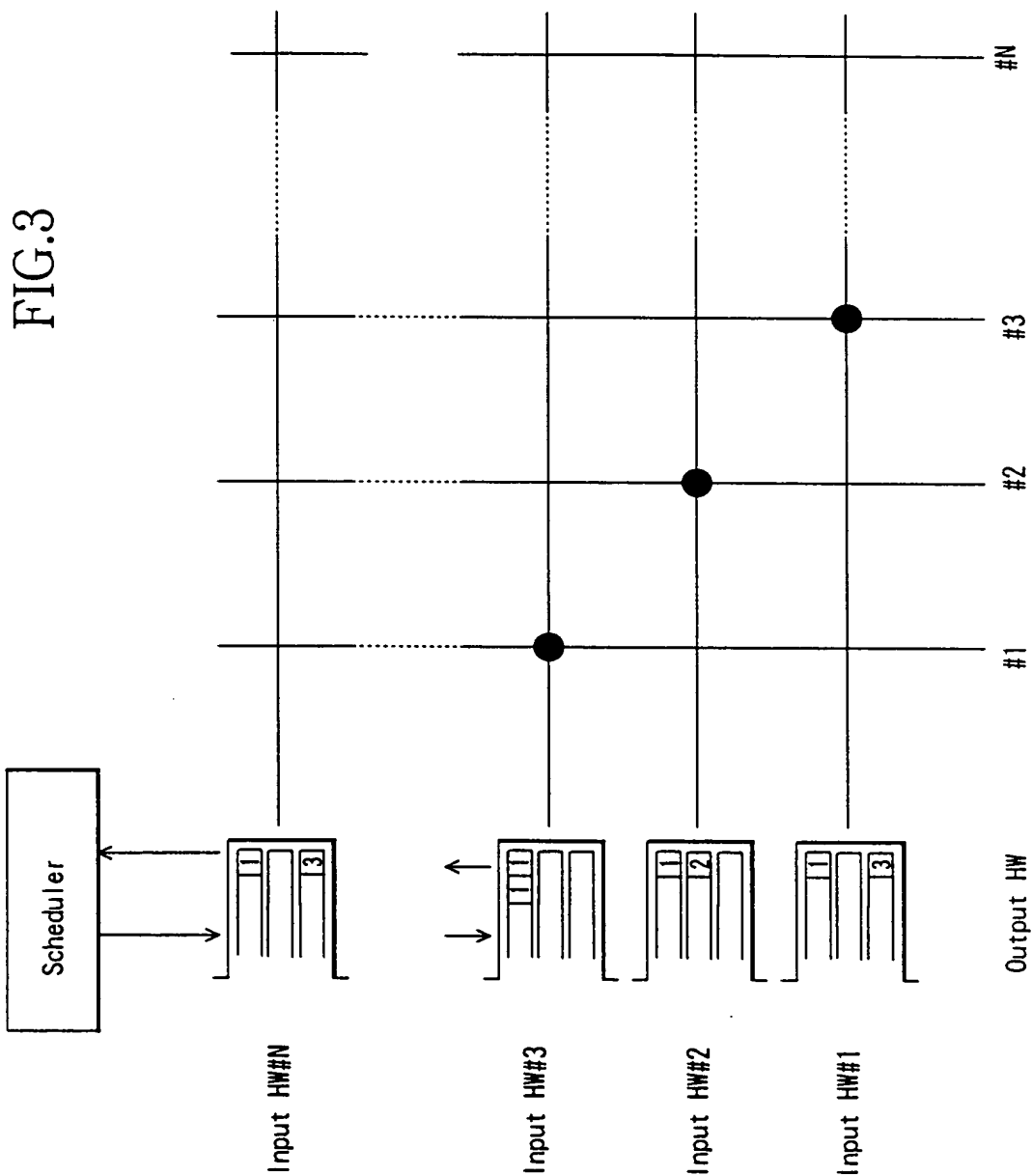


FIG. 4

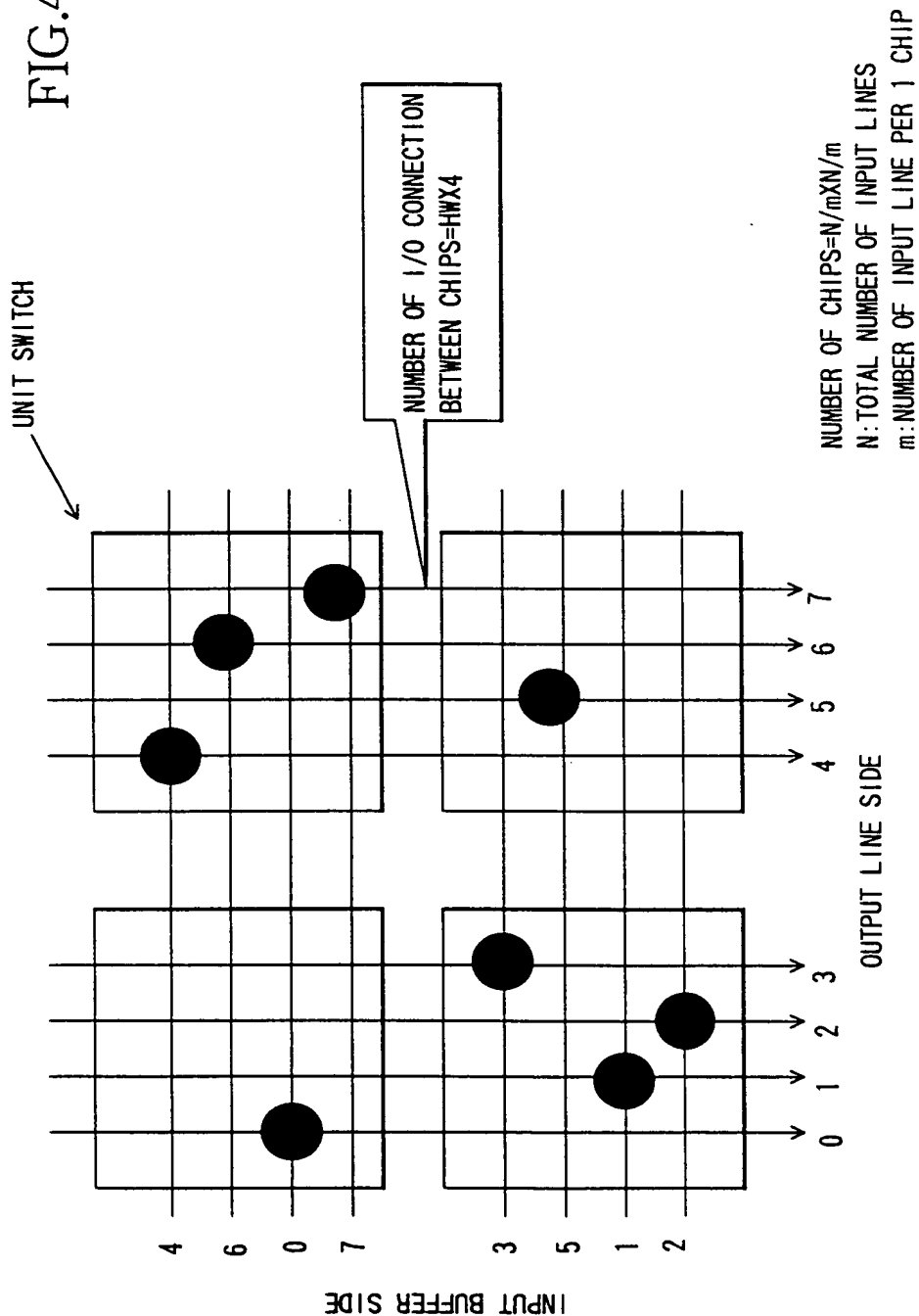


FIG. 5

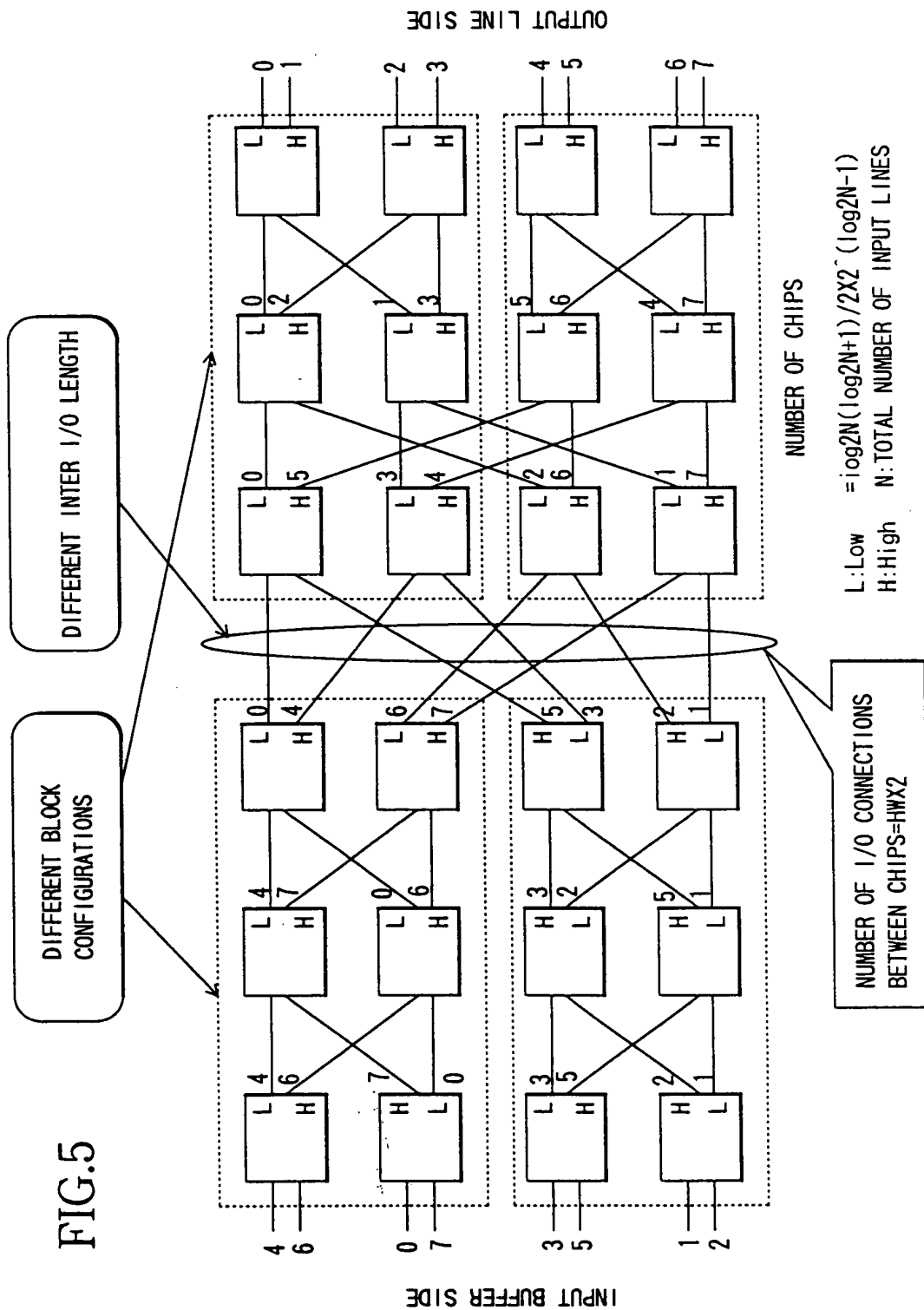


FIG.6

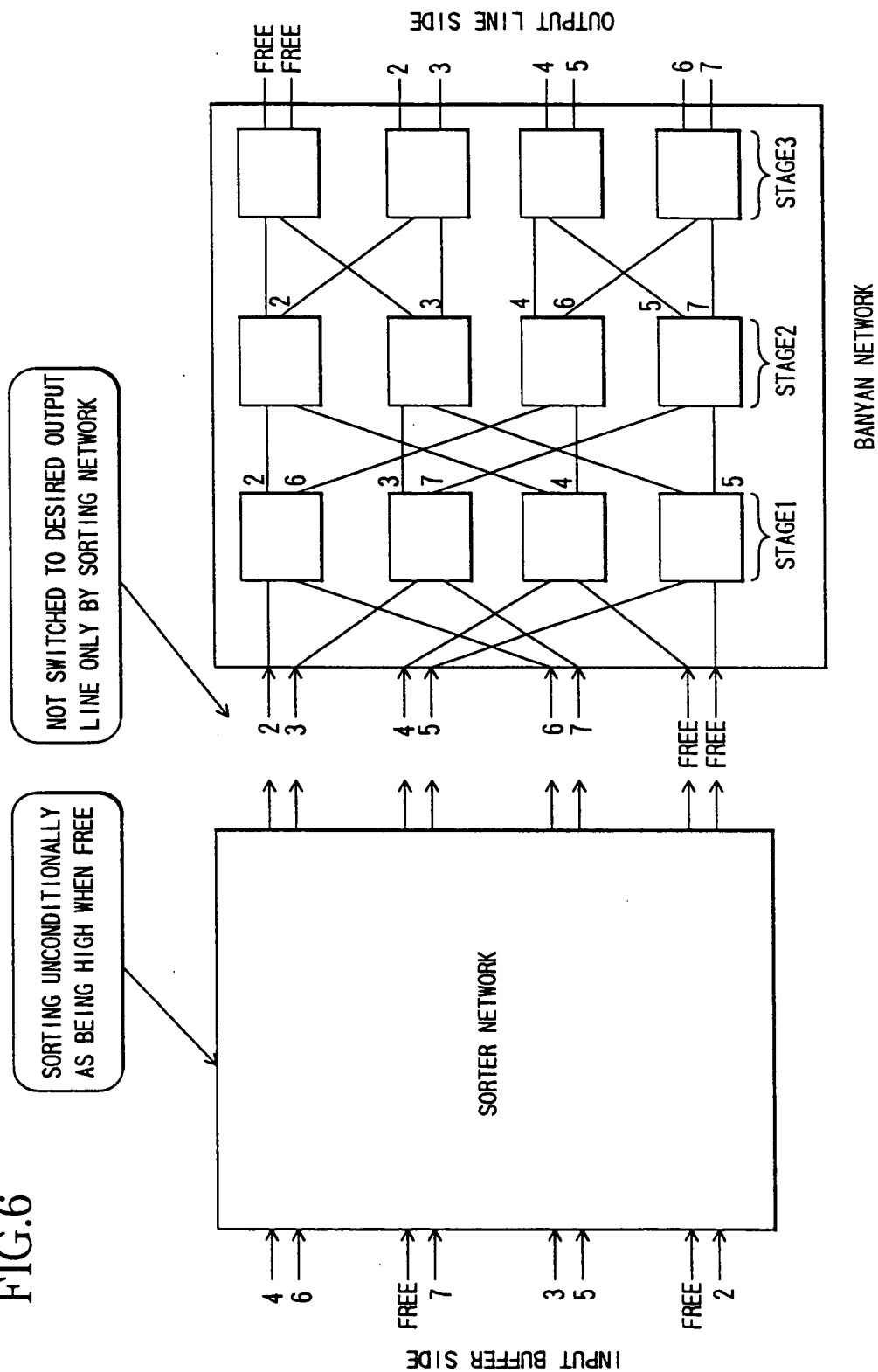


FIG.7

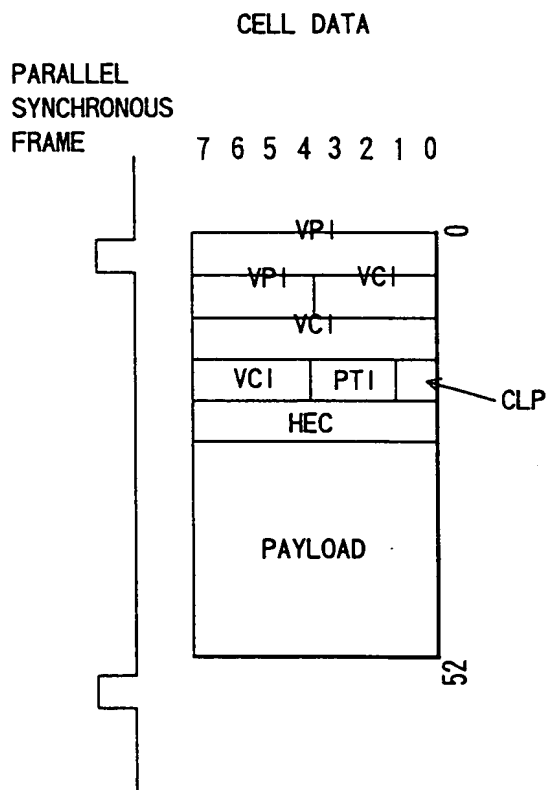
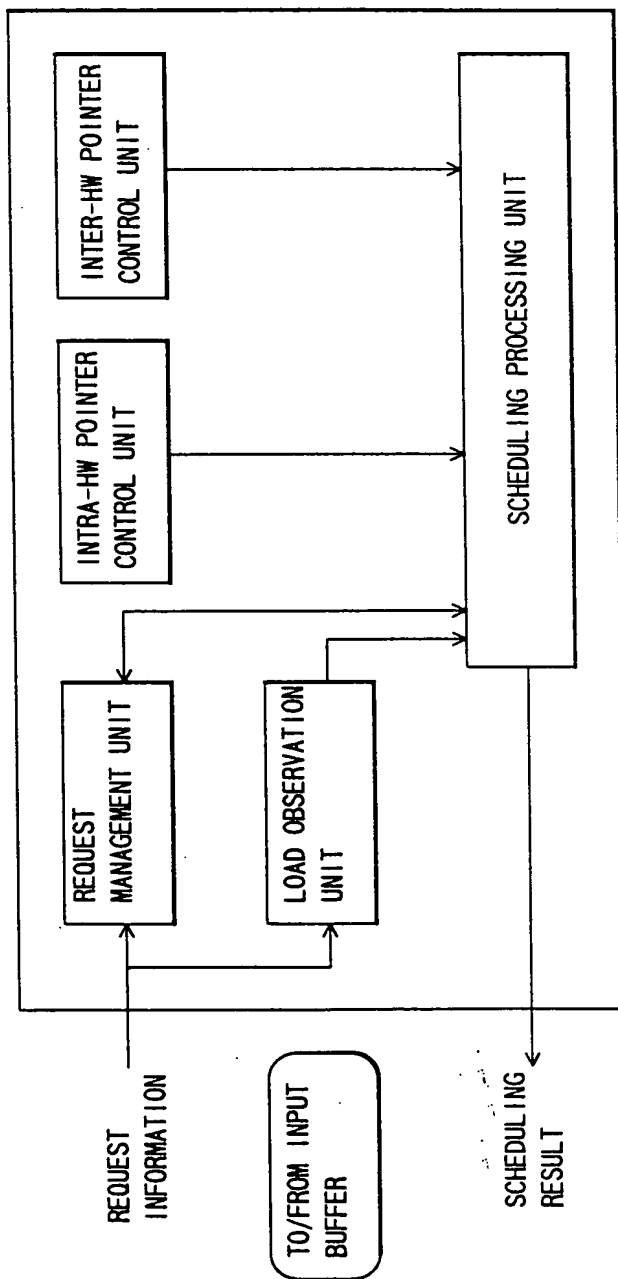


FIG.8



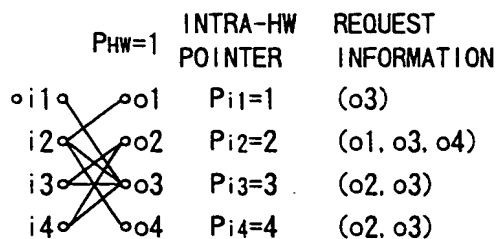


FIG. 9(a) INITIAL STATE (STEP0)

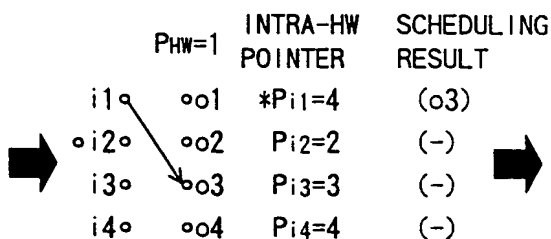


FIG. 9(b) AFTER STEP1

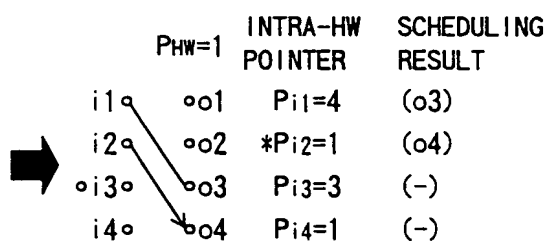


FIG. 9(c) AFTER STEP2

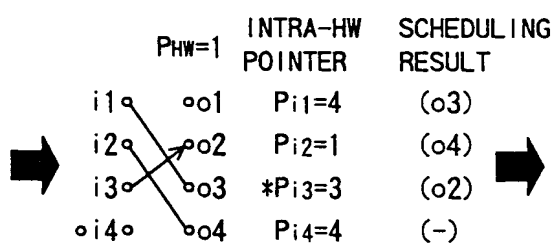


FIG. 9(d) AFTER STEP3

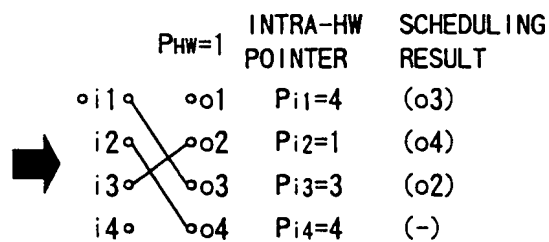


FIG. 9(e) AFTER STEP4

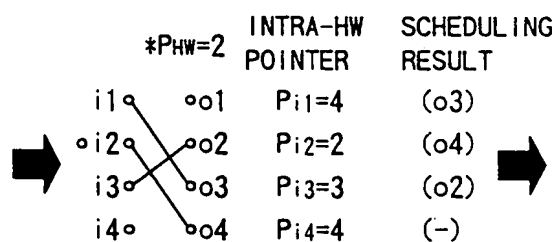


FIG. 9(f) AFTER STEP5

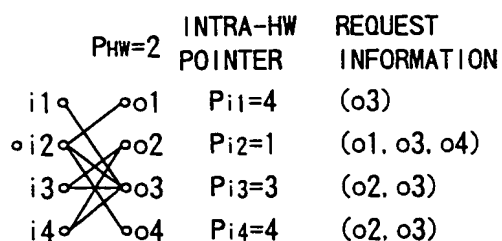


FIG. 10(a) INITIAL STATE (STEP0)

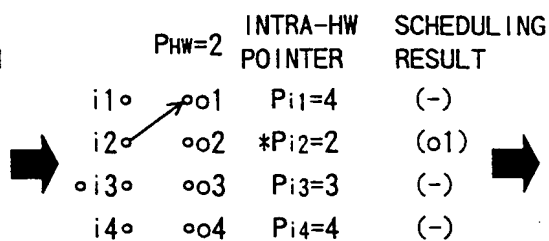


FIG. 10(b) AFTER STEP1

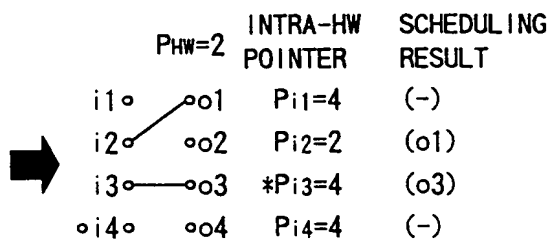


FIG. 10(c) AFTER STEP2

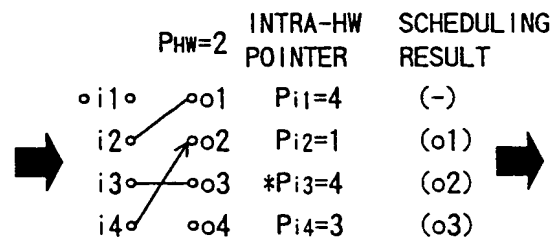


FIG. 10(d) AFTER STEP3

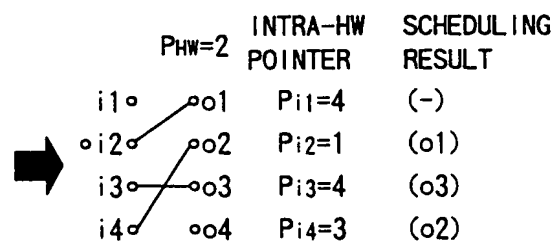


FIG. 10(e) AFTER STEP4

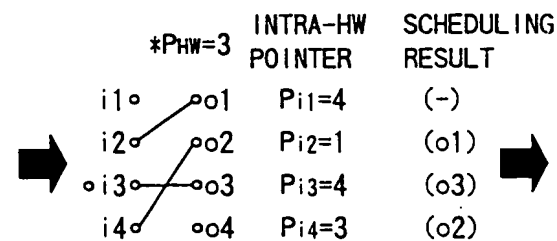


FIG. 10(f) AFTER STEP5

FIG.11

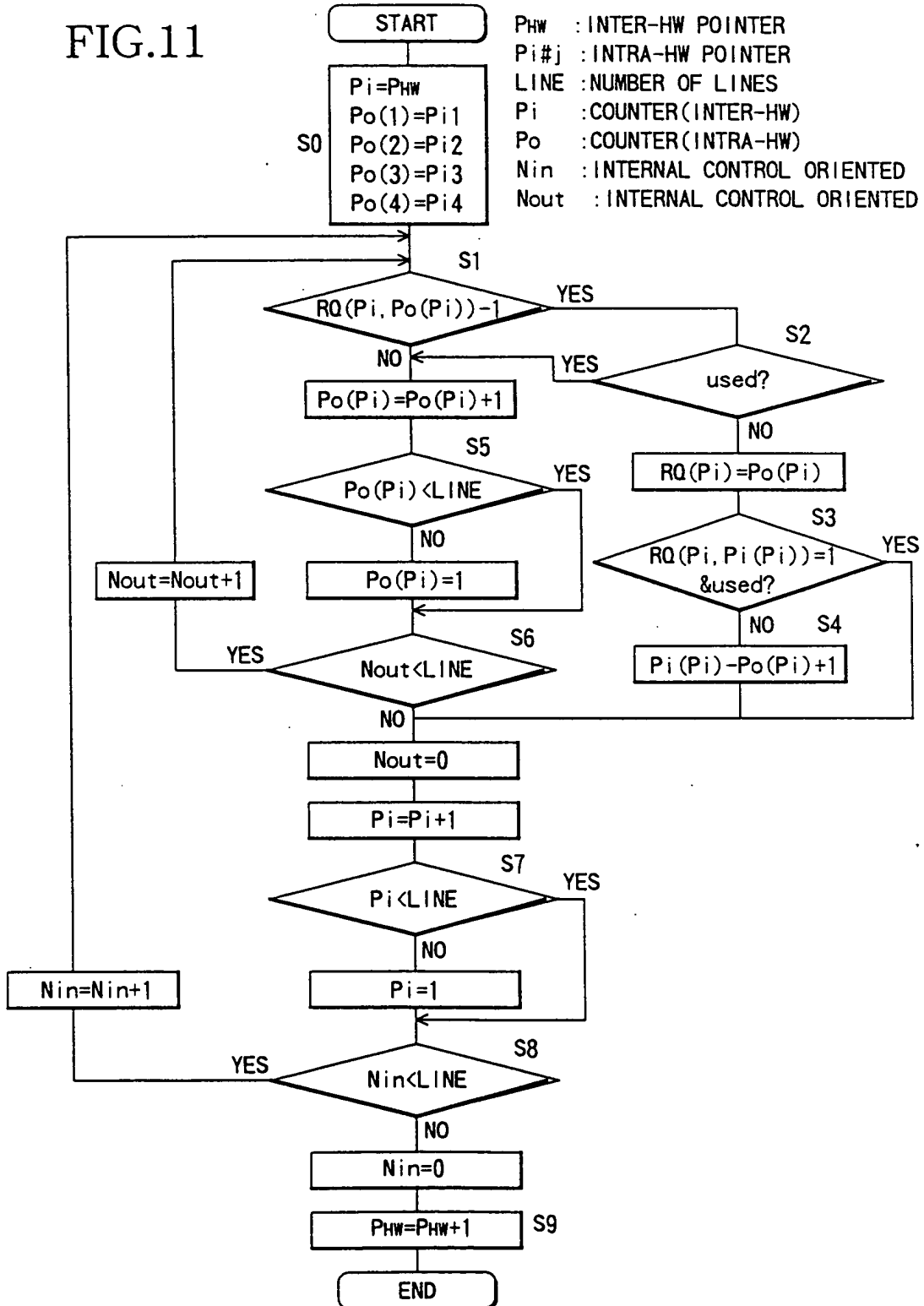
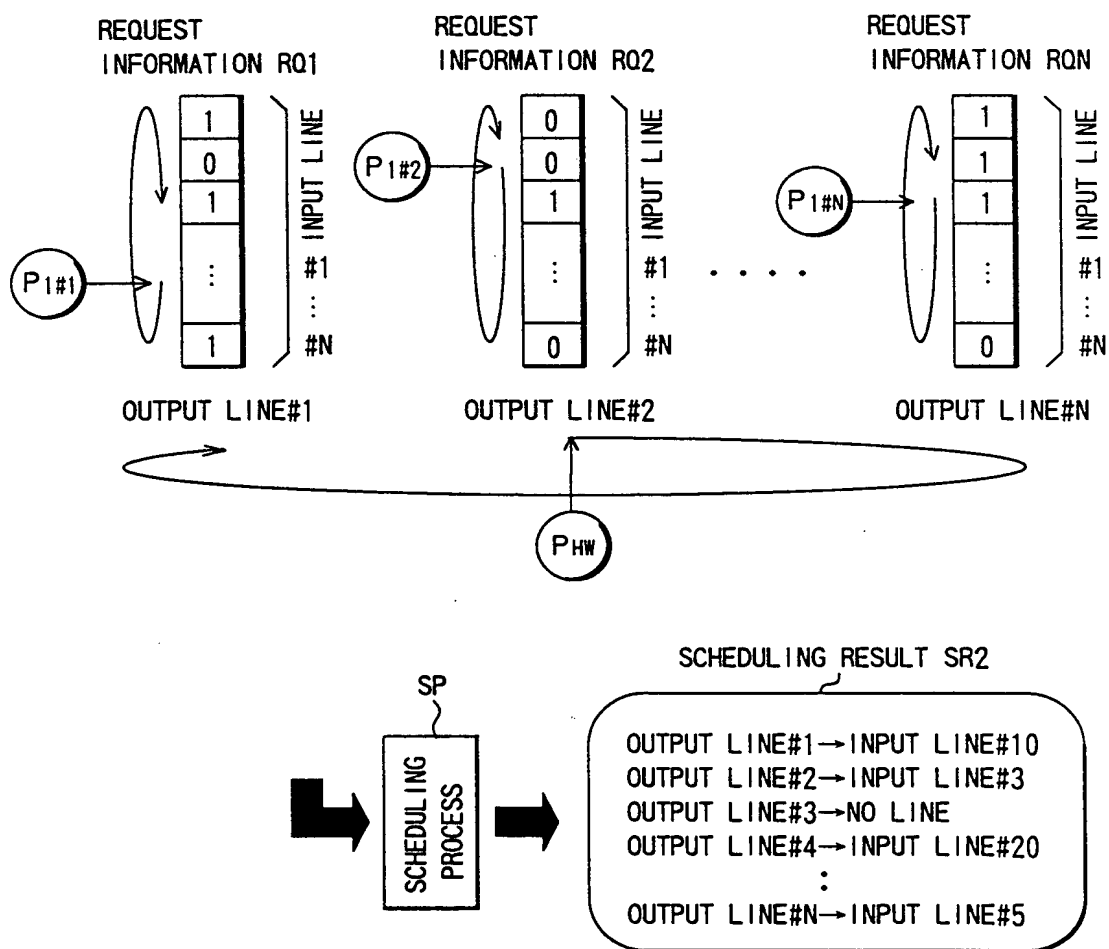


FIG.12



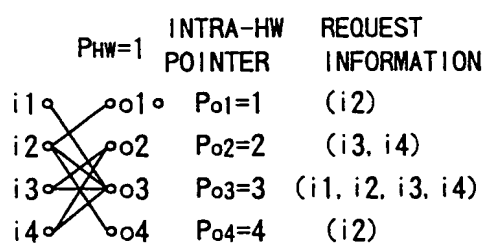


FIG. 13(a) INITIAL STATE (STEP0)

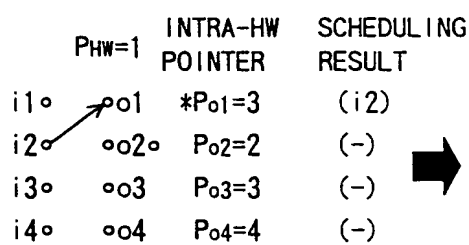


FIG. 13(b) AFTER STEP1

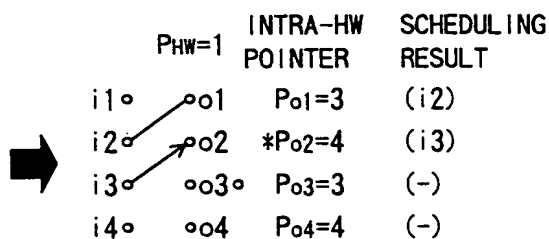


FIG. 13(c) AFTER STEP2

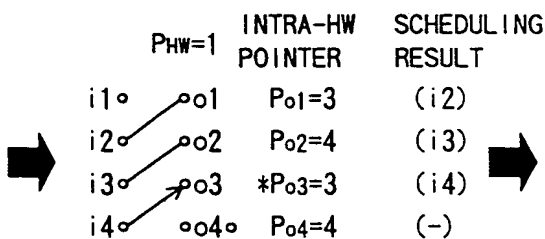


FIG. 13(d) AFTER STEP3

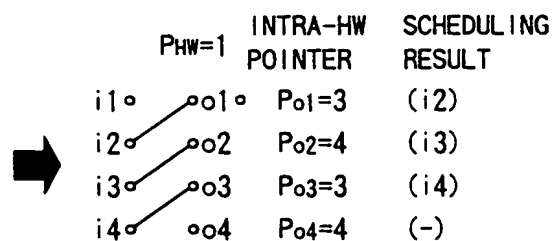


FIG. 13(e) AFTER STEP4

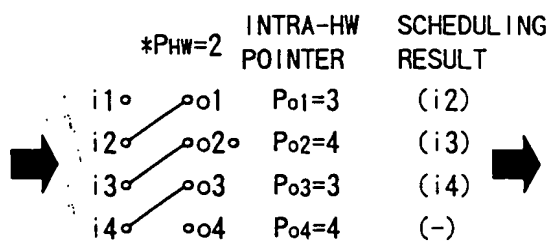


FIG. 13(f) AFTER STEP5

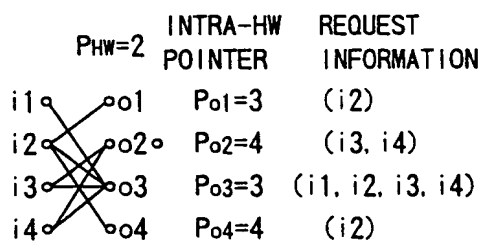


FIG. 14(a) INITIAL STATE (STEP0)

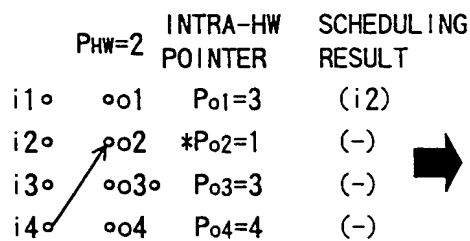


FIG. 14(b) AFTER STEP1

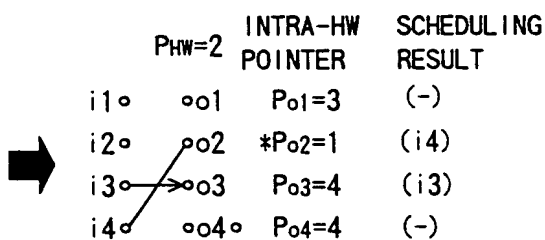


FIG. 14(c) AFTER STEP2

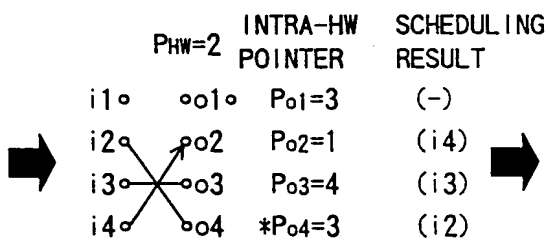


FIG. 14(d) AFTER STEP3

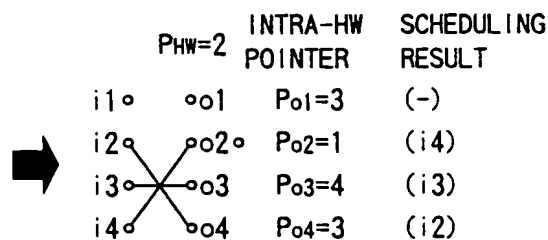


FIG. 14(e) AFTER STEP4

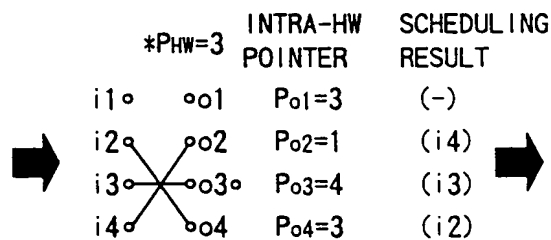


FIG. 14(f) AFTER STEP5

FIG.15

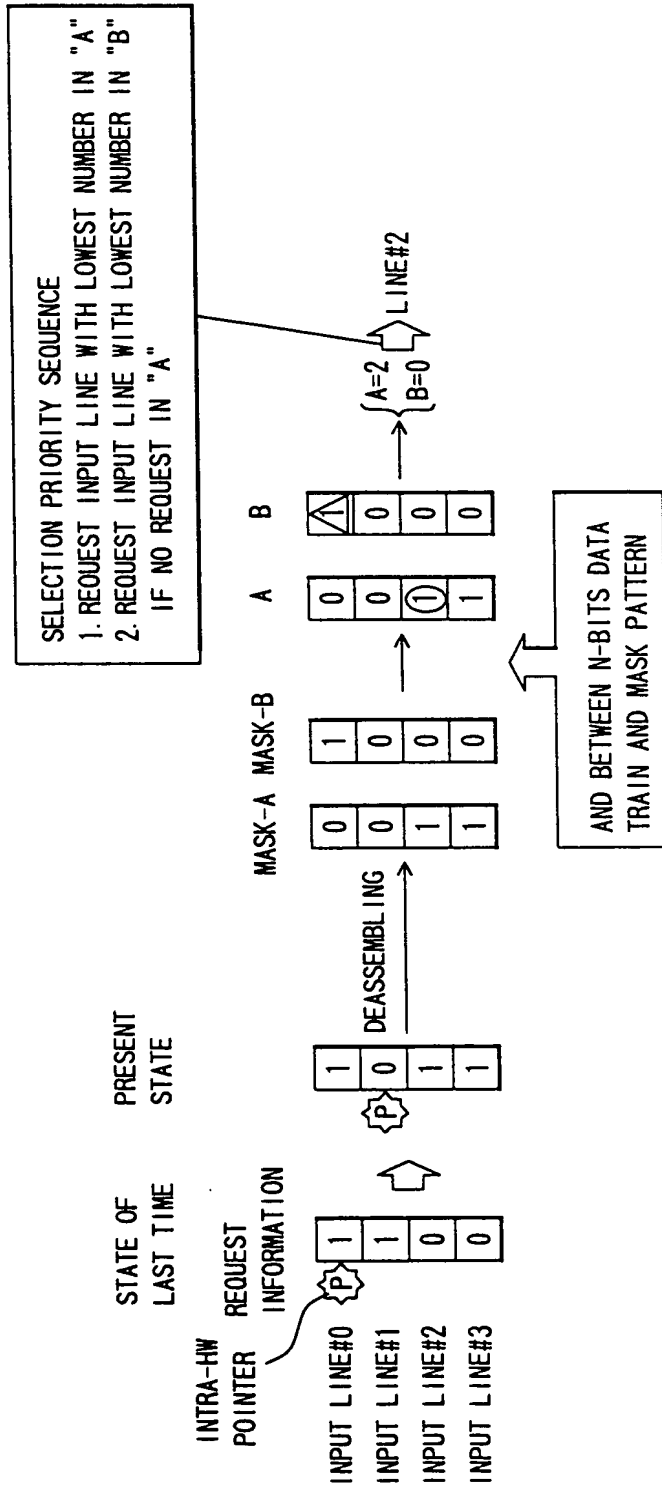


FIG.16

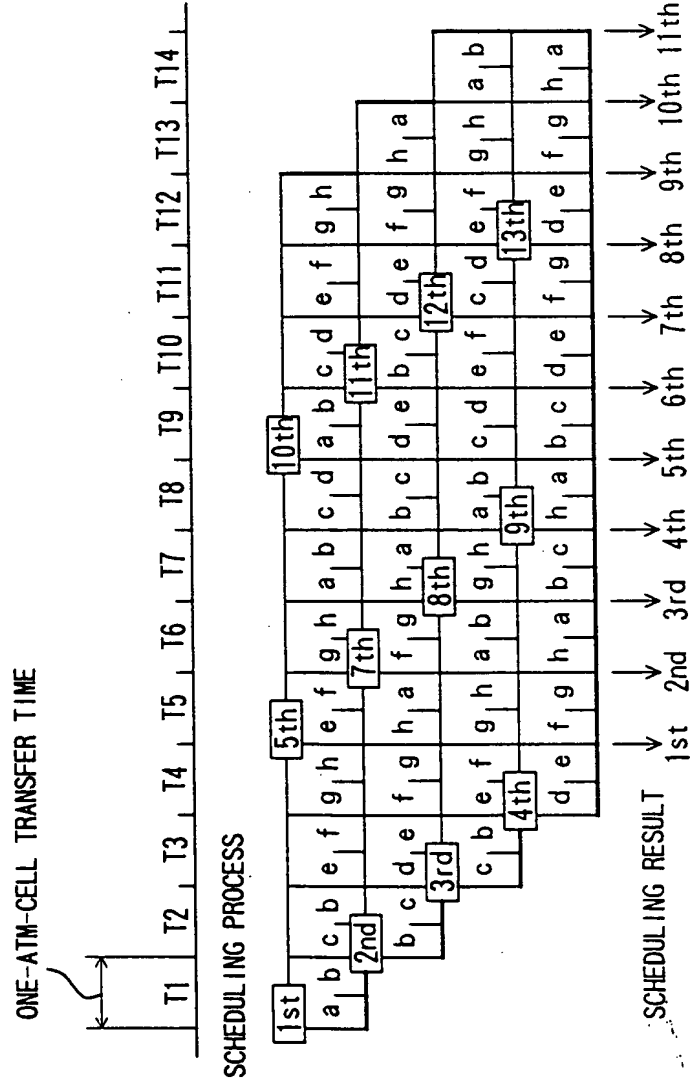
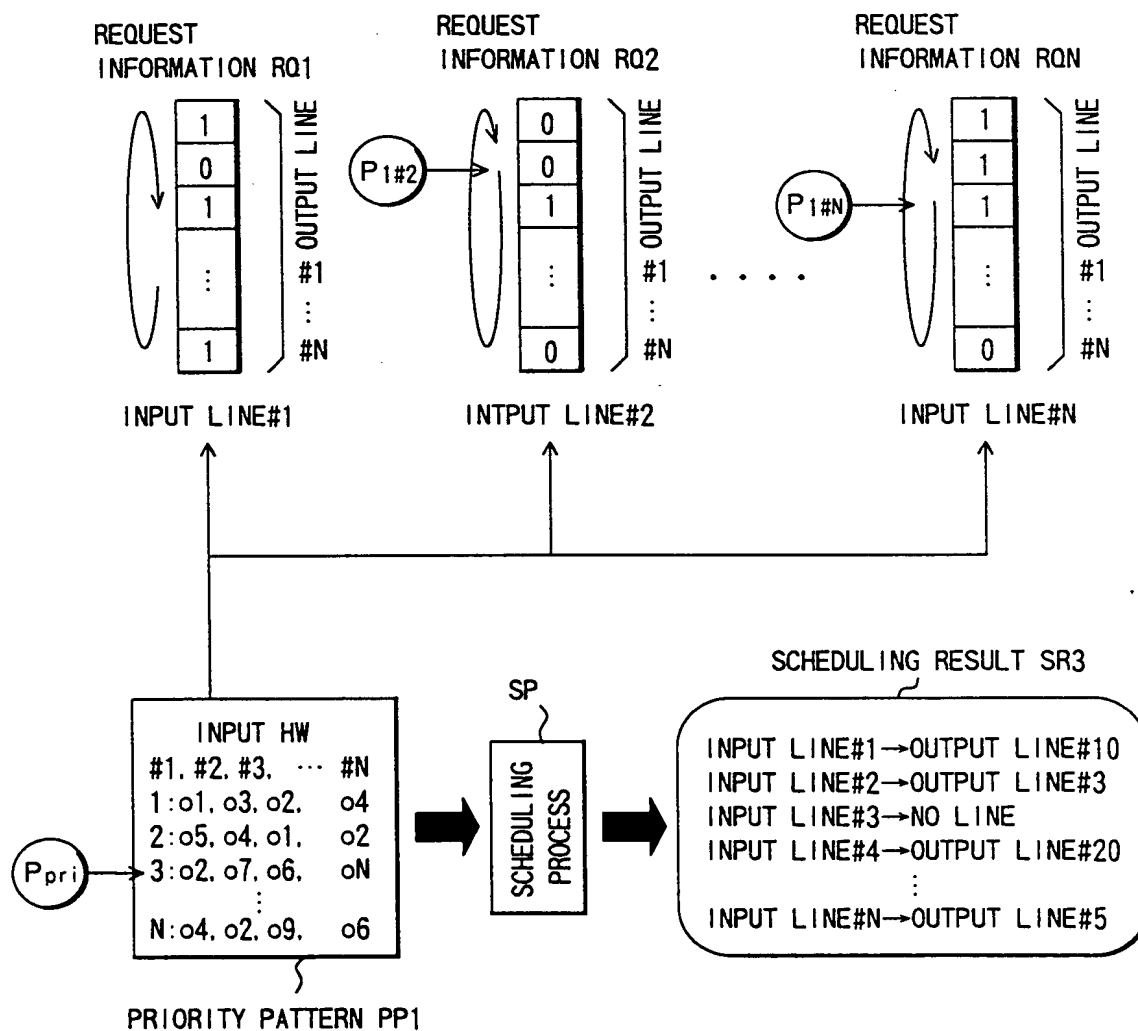


FIG.17



	PRIORITY					REQUEST INFORMATION
	Ppri=1	1 st	2 nd	3 rd	4 th	
i1	o1	o1	o3	o2	o4	(o3)
i2	o2	o4	o2	o1	o3	(o1, o2)
i3	o3	o3	o1	o4	o2	(o2, o4)
i4	o4	o2	o4	o3	o1	(o2, o3)

FIG. 18(a) INITIAL STATE
(STEP0)

	PRIORITY					SCHEDULING RESULT
	Ppri=1	1 st	2 nd	3 rd	4 th	
i1	o1	o1	o3	o2	o4	(-)
i2	o2	o4	o2	o1	o3	(-)
i3	o3	o3	o1	o4	o2	(-)
i4	o4	*o2	o4	o3	o1	(o2)

FIG. 18(b) AFTER STEP1

	PRIORITY					SCHEDULING RESULT
	Ppri=1	1 st	2 nd	3 rd	4 th	
i1	o1	*o1	o3	o2	o4	(o3)
i2	o2	o4	o2	o1	o3	(-)
i3	o3	*o3	o1	o4	o2	(o1)
i4	o4	o2	o4	o3	o1	(o2)

FIG. 18(c) AFTER STEP2

	PRIORITY					SCHEDULING RESULT
	Ppri=1	1 st	2 nd	3 rd	4 th	
i1	o1	o1	o3	o2	o4	(o3)
i2	o2	o4	o2	o1	o3	(-)
i3	o3	o3	o1	o4	o2	(o1)
i4	o4	o2	o4	o3	o1	(o2)

FIG. 18(d) AFTER STEP3

	PRIORITY					SCHEDULING RESULT
	Ppri=1	1 st	2 nd	3 rd	4 th	
i1	o1	o1	o3	o2	o4	(o3)
i2	o2	o4	o2	o1	o3	(-)
i3	o3	o3	o1	o4	o2	(o1)
i4	o4	o2	o4	o3	o1	(o2)

FIG. 18(e) AFTER STEP4

	PRIORITY					SCHEDULING RESULT
	*Ppri=1	1 st	2 nd	3 rd	4 th	
i1	o1	o1	o3	o2	o4	(o3)
i2	o2	o4	o2	o1	o3	(-)
i3	o3	o3	o1	o4	o2	(o1)
i4	o4	o2	o4	o3	o1	(o2)

FIG. 18(f) AFTER STEP5

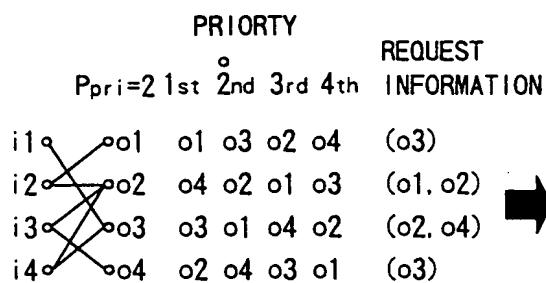


FIG. 19(a) INITIAL STATE (STEP0)

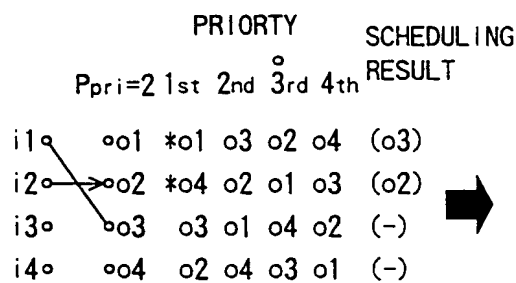


FIG. 19(b) AFTER STEP1

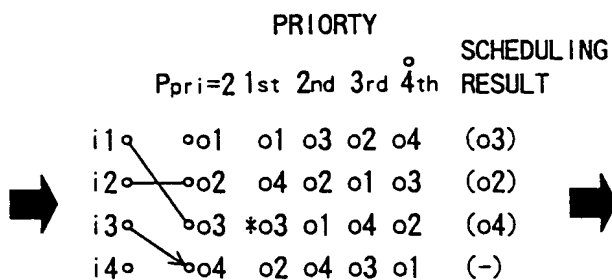


FIG. 19(c) AFTER STEP2

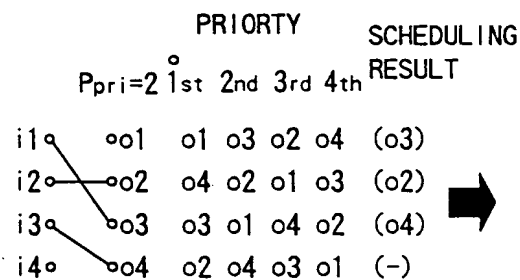


FIG. 19(d) AFTER STEP3

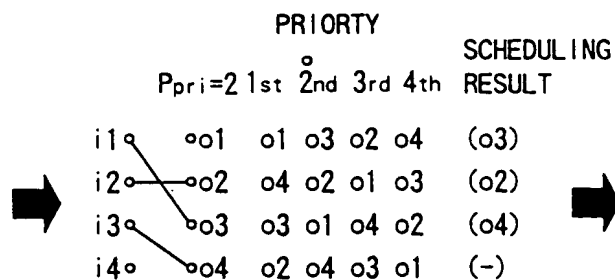


FIG. 19(e) AFTER STEP4

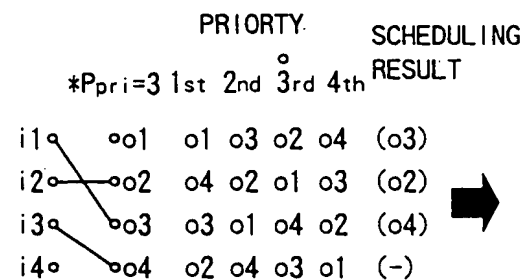


FIG. 19(f) AFTER STEP5

FIG.20

Ppri : PRIORITY POINTER
Pno : COUNTER (PRIORITY PATTERN No.)
LINE : NUMBER OF LINES
PT : PRIORITY PATTERN VALUE
i : INTERNAL CONTROL ORIENTED
Nno : INTERNAL CONTROL ORIENTED

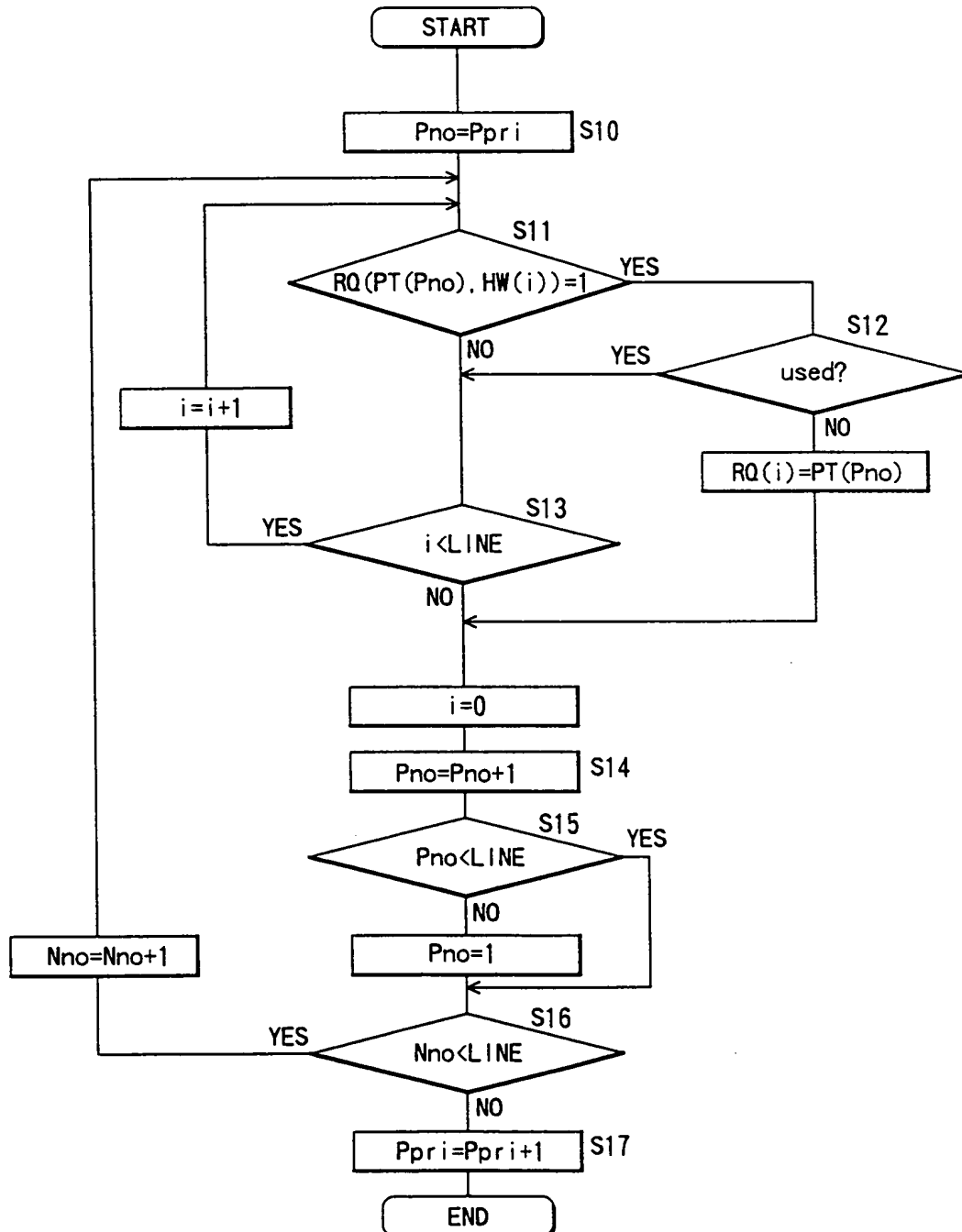
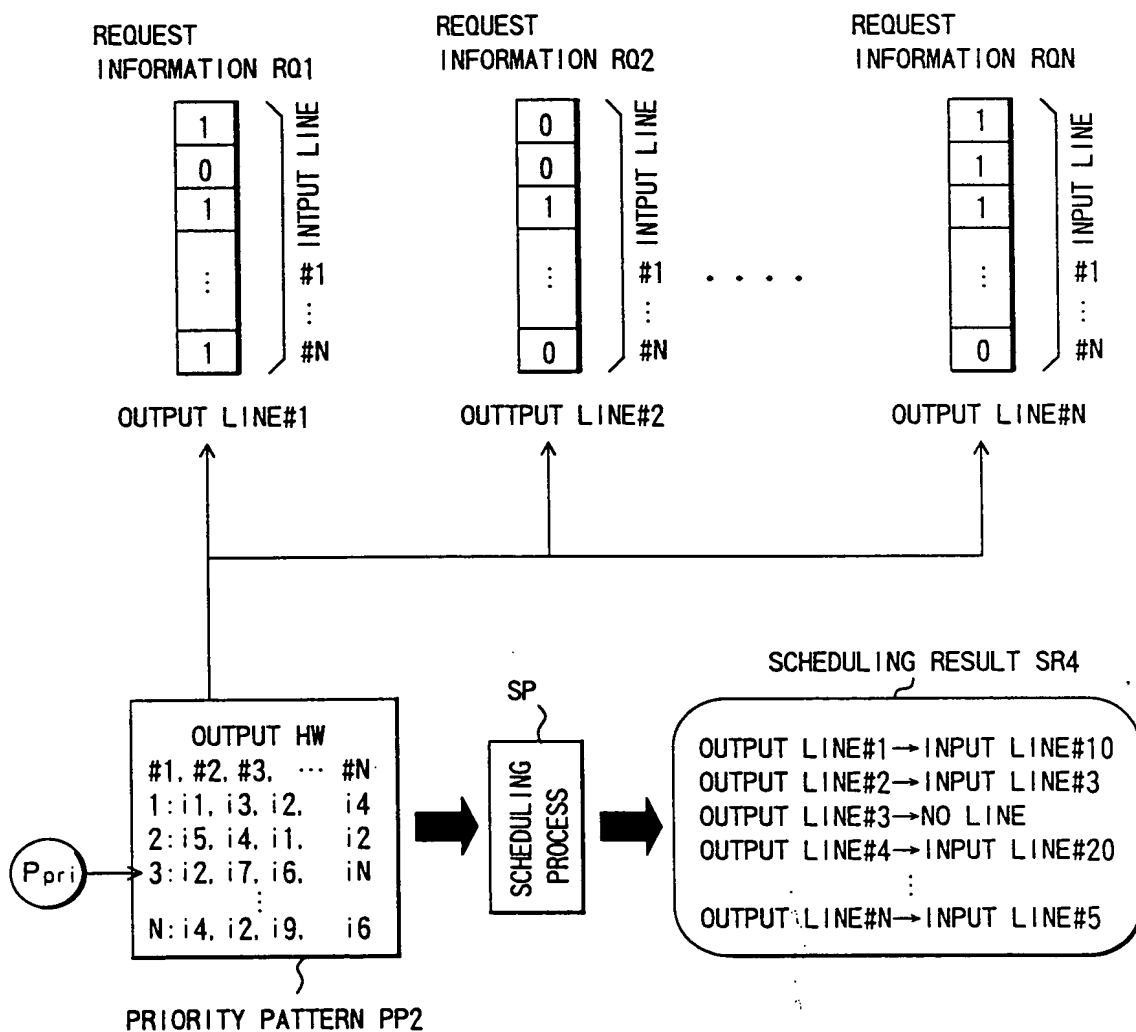


FIG.21



PRIORITY					REQUEST INFORMATION
Ppri=1	1 st	2 nd	3 rd	4 th	
i1	o1	i1	i3	i2	(i2)
i2	o2	i4	i2	i1	(i2, i3, i4)
i3	o3	i3	o1	i4	(i2, i4)
i4	o4	i2	i4	i3	(i3)

FIG. 22(a) INITIAL STATE (STEP0)

PRIORITY					SCHEDULING RESULT
Ppri=1	1 st	2 nd	3 rd	4 th	
i1	o1	i1	i3	i2	(-)
i2	o2	*i4	i2	i1	(i4)
i3	o3	i3	i1	i4	(-)
i4	o4	i2	i4	i3	(-)

FIG. 22(b) AFTER STEP1

PRIORITY					SCHEDULING RESULT
Ppri=1	1 st	2 nd	3 rd	4 th	
i1	o1	*i1	i3	i2	(i3)
i2	o2	i4	i2	i1	(i4)
i3	o3	*i3	i1	i4	(i1)
i4	o4	i2	i4	i3	(-)

FIG. 22(c) AFTER STEP3

PRIORITY					SCHEDULING RESULT
Ppri=1	1 st	2 nd	3 rd	4 th	
i1	o1	i1	i3	i2	(i3)
i2	o2	i4	i2	i1	(i4)
i3	o3	i3	i1	i4	(i1)
i4	o4	i2	i4	i3	(-)

FIG. 22(d) AFTER STEP4

PRIORITY					SCHEDULING RESULT
Ppri=1	1 st	2 nd	3 rd	4 th	
i1	o1	i1	i3	i2	(i3)
i2	o2	i4	i2	i1	(i4)
i3	o3	i3	i1	i4	(i1)
i4	o4	i2	i4	i3	(-)

FIG. 22(e) AFTER STEP4

PRIORITY					SCHEDULING RESULT
*Ppri=1	1 st	2 nd	3 rd	4 th	
i1	o1	i1	i3	i2	(i3)
i2	o2	i4	i2	i1	(i4)
i3	o3	i3	i1	i4	(i1)
i4	o4	i2	i4	i3	(-)

FIG. 22(f) AFTER STEP5

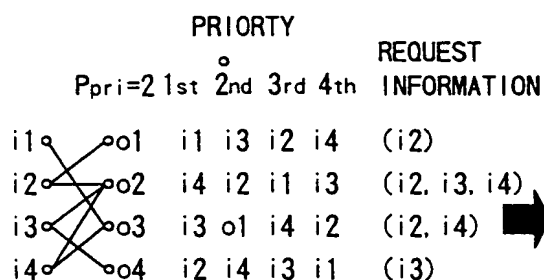


FIG. 23(a) INITIAL STATE (STEP0)

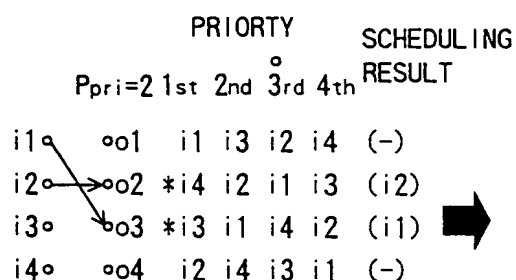


FIG. 23(b) AFTER STEP1

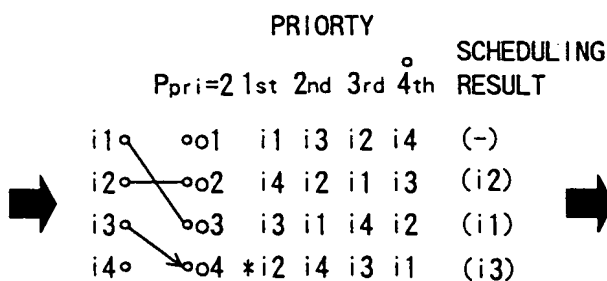


FIG. 23(c) AFTER STEP3

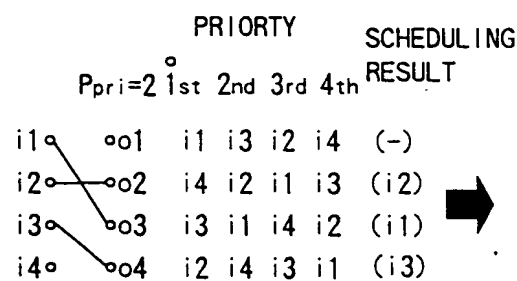


FIG. 23(d) AFTER STEP4

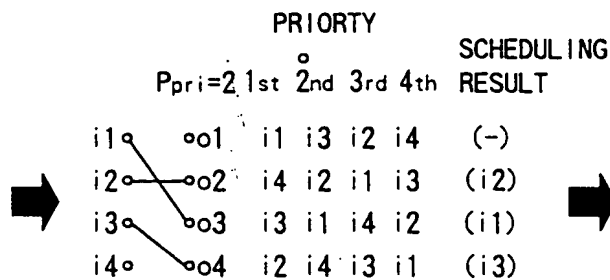


FIG. 23(e) AFTER STEP4

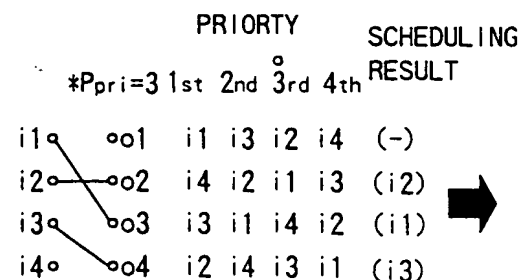


FIG. 23(f) AFTER STEP5

FIG.24

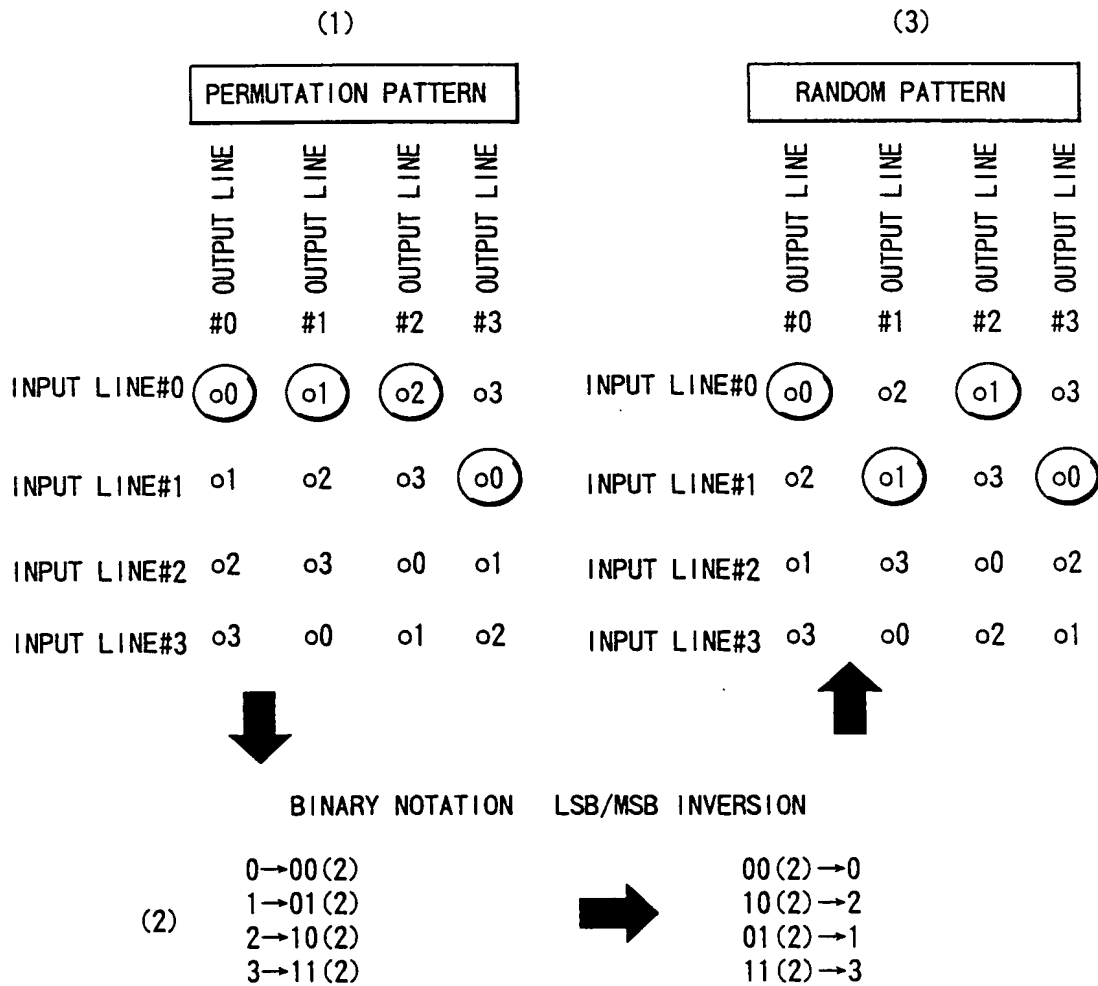


FIG.25

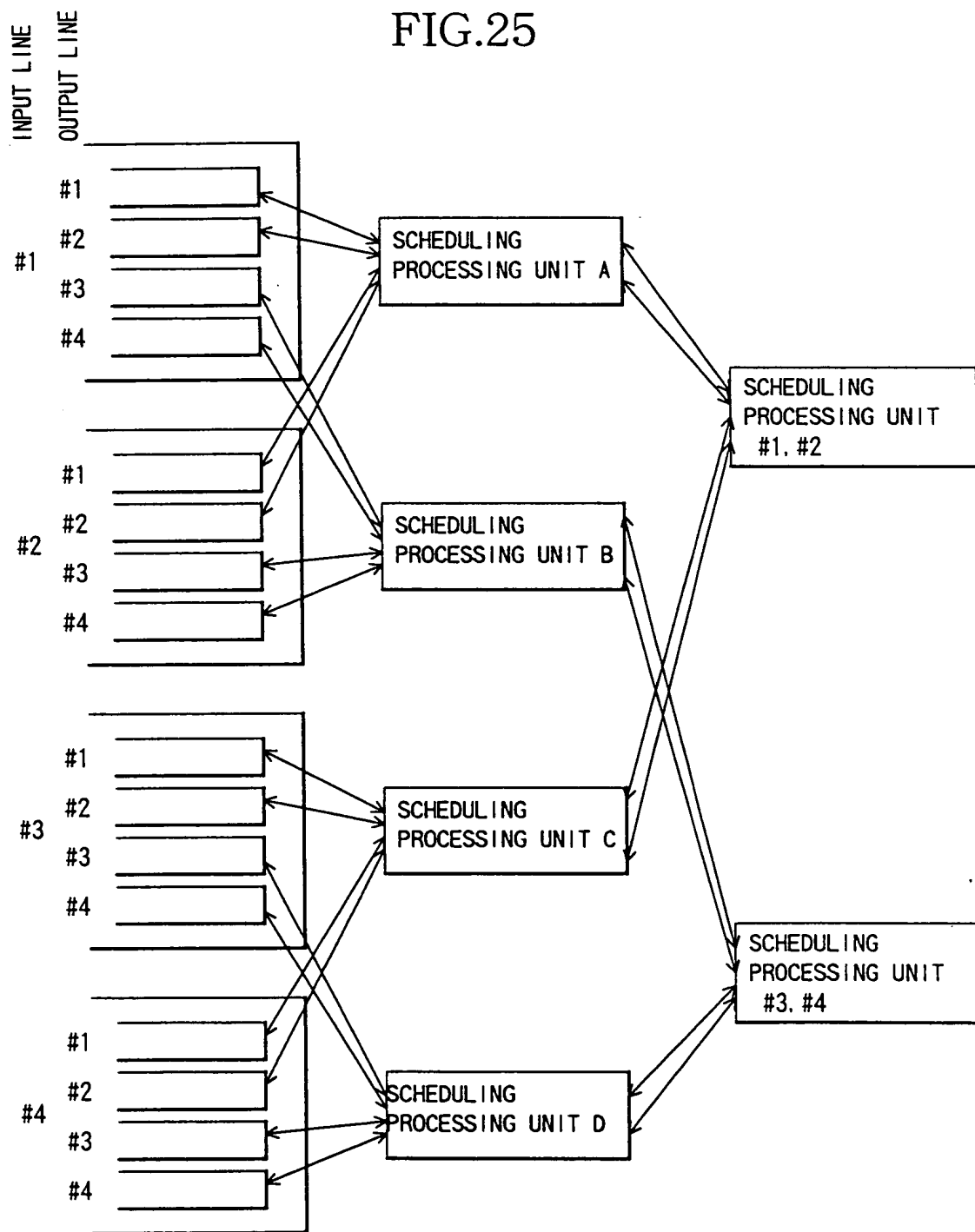


FIG.26 (a)

TENTATIVE CANDIDATE SELECTION IN SCHEDULING PROCESSING UNIT A

	PRIORITY		SCHEDULING RESULT			PRIORITY		SCHEDULING RESULT
	1st	2nd				1st	2nd	
i1 — o1	o1	o2	(o1)	➡		i1 —> o1	o1 o2	(o1)
i2 — o2	o2	o1	(o2)			i2 —> o2	o2 o1	(o2)

TENTATIVE CANDIDATE SELECTION IN SCHEDULING PROCESSING UNIT B

	PRIORITY		SCHEDULING RESULT			PRIORITY		SCHEDULING RESULT
	1st	2nd				1st	2nd	
i1 — o3	o3	o4	(o3)	➡		i1 —> o3	o3 o4	(o3)
i2 — o4	o4	o3	(-)			i2 — o4	o4 o3	(-)

TENTATIVE CANDIDATE SELECTION IN SCHEDULING PROCESSING UNIT C

	PRIORITY		SCHEDULING RESULT			PRIORITY		SCHEDULING RESULT
	1st	2nd				1st	2nd	
i3 — o1	o1	o2	(-)	➡		i3 — o1	o1 o2	(-)
i4 — o2	o2	o1	(-)			i4 — o2	o2 o1	(-)

TENTATIVE CANDIDATE SELECTION IN SCHEDULING PROCESSING UNIT D

	PRIORITY		SCHEDULING RESULT			PRIORITY		SCHEDULING RESULT
	1st	2nd				1st	2nd	
i3 — o3	o3	o4	(o3)	➡		i3 —> o3	o3 o4	(o3)
i4 — o4	o4	o3	(o3)			i4 — o4	o4 o3	(-)

FIG.26 (b)

	PRIORITY				SCHEDULING RESULT			PRIORITY				SCHEDULING RESULT
	1st	2nd	3rd	4th				1st	2nd	3rd	4th	
i1 — o1	o1	o3	o2	o4	(o1, o3)	➡		i1 —> o1	o3 o4 o1 o2			(o1)
i2 — o2	o2	o1	o4	o3	(o2)			i2 —> o2	o4 o3 o2 o1			(o2)
i3 — o3	o3	o4	o1	o2	(o3)			i3 —> o3	o1 o2 o3 o4			(o3)
i4 — o4	o4	o3	o2	o1	(-)			i4 — o4	o2 o1 o4 o3			(-)



FIG.29

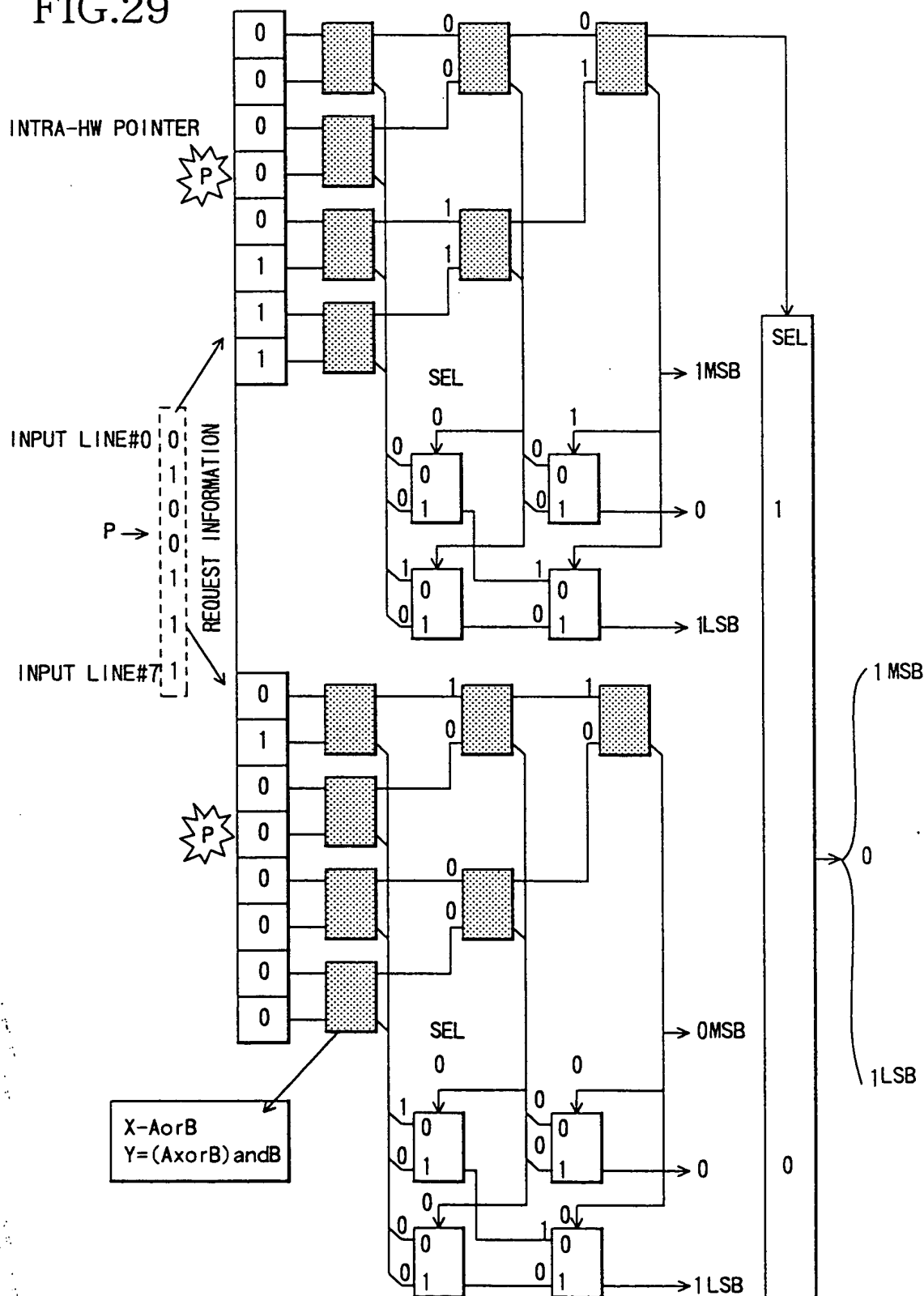


FIG.32

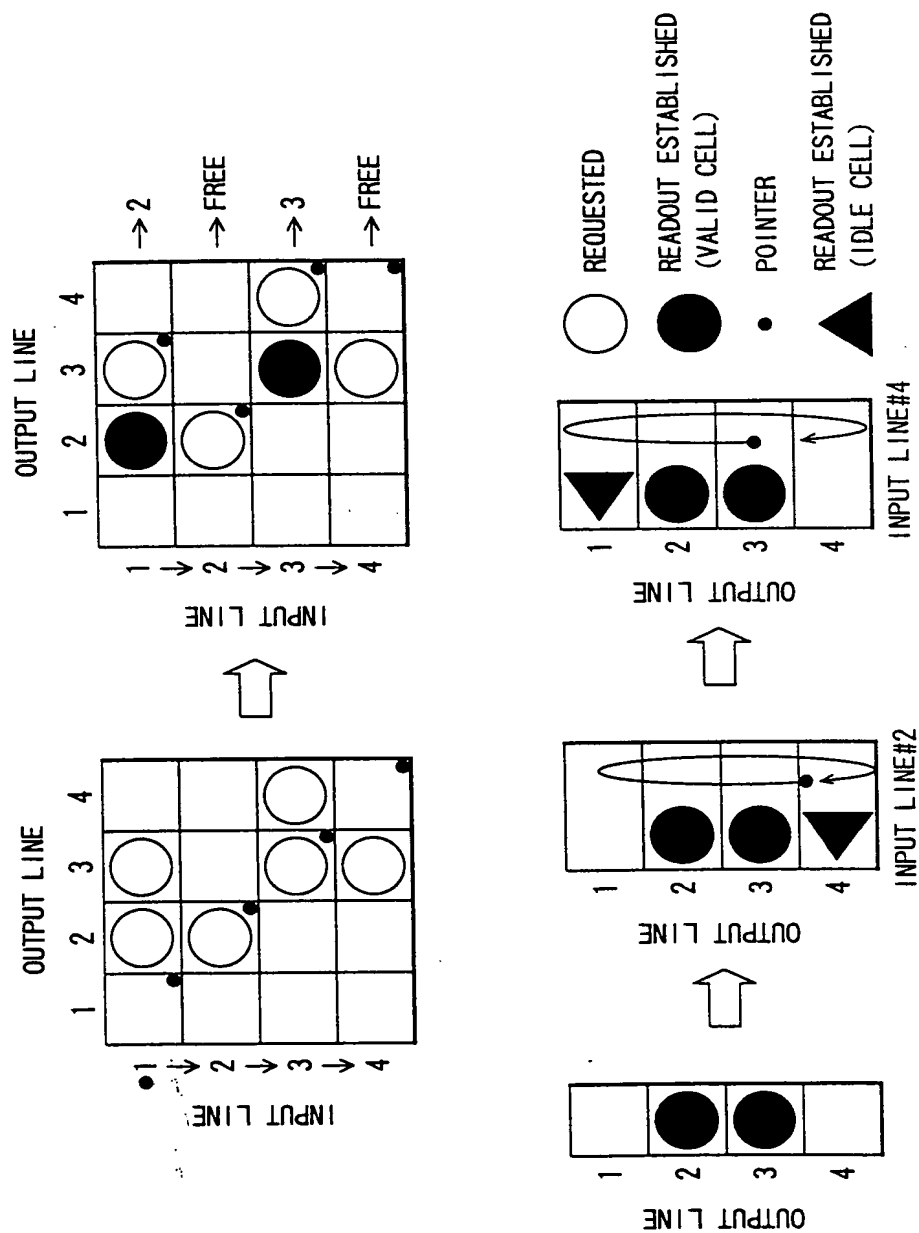


FIG.33

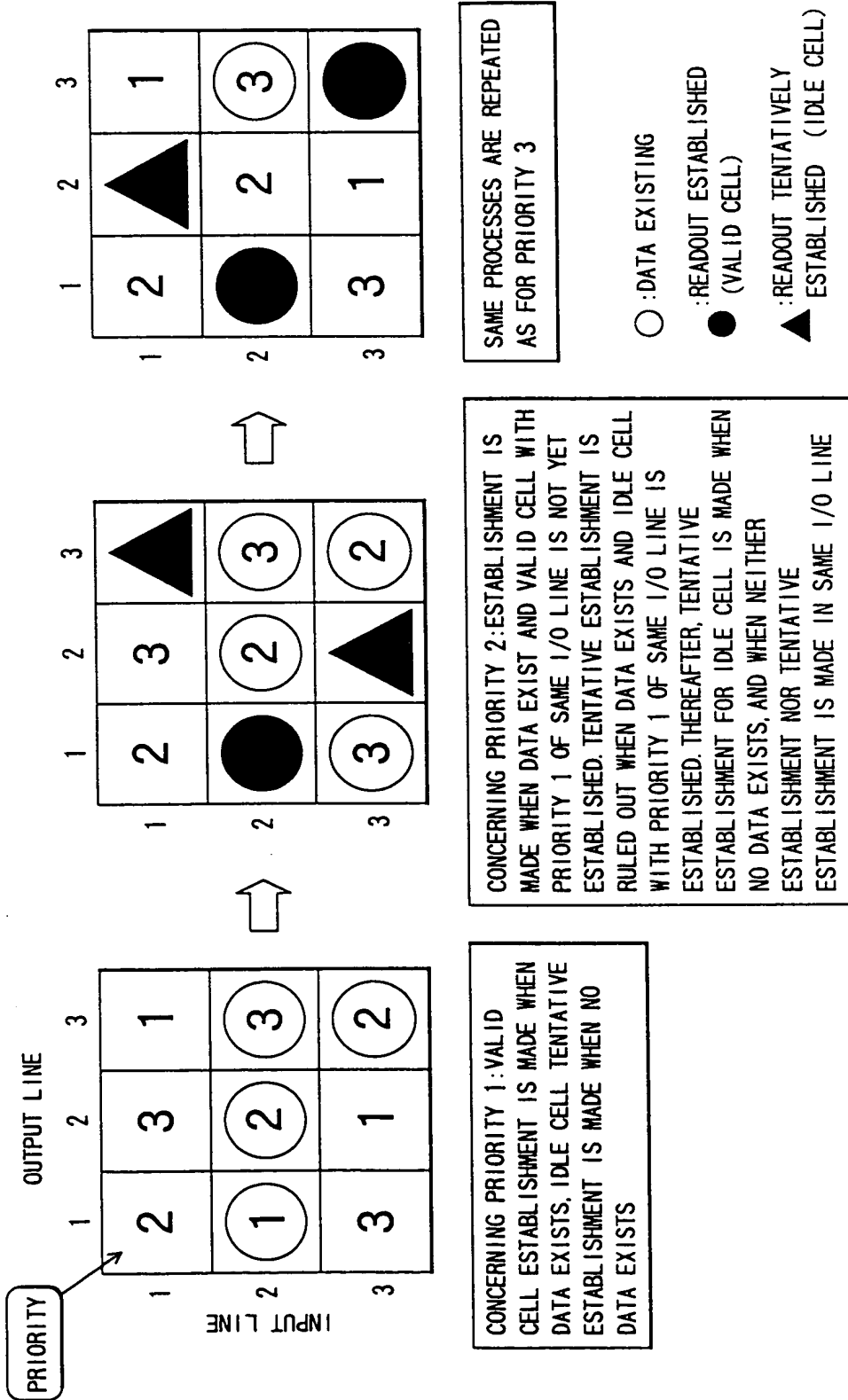


FIG.35

	SCHEDULER UNIT	INPUT LINE NUMBER	DELAY COMPONENT (INPUT BUFFER)	INPUT TO SW
T=0	8 7 6 5 4 3 2 1 3 2 1 3 2 1 3 2	#3	3	
	8 7 6 5 4 3 2 1 1 3 2 1 3 2 1 3	#2	2	
	8 7 6 5 4 3 2 1 2 1 3 2 1 3 2 1	#1	1	
T=1	9 8 7 6 5 4 3 2 1 3 2 1 3 2 1 3	#3	3	
	9 8 7 6 5 4 3 2 2 1 3 2 1 3 2 1	#2	2	
	9 8 7 6 5 4 3 2 3 2 1 3 2 1 3 2	#1	1	1 START OF PHASE ADJUSTMENT $\Delta T=0, SW=1$
T=2	10 9 8 7 6 5 4 3 2 1 3 2 1 3 2 1	#3	3	
	10 9 8 7 6 5 4 3 3 2 1 3 2 1 3 2	#2	2	1 3
	10 9 8 7 6 5 4 3 1 3 2 1 3 2 1 3	#1	1	2 2 $\Delta T=1, SW=1$
T=3	11 10 9 8 7 6 5 4 3 2 1 3 2 1 3 2	#3	3	1 2
	11 10 9 8 7 6 5 4 1 3 2 1 3 2 1 3	#2	2	2 1 PHASE ADJUSTMENT $=\Delta SW - \Delta T = -1$
	11 10 9 8 7 6 5 4 2 1 3 2 1 3 2 1	#1	1	3 3 $\Delta T=2, SW=1, \Delta SW=2-1=1$
T=4	12 11 10 9 8 7 6 5 1 3 2 1 3 2 1 3	#3	3	2 3
	12 11 10 9 8 7 6 5 2 1 3 2 1 3 2 1	#2	1=2-1	4 3 DISCARD CELL WHEN REDUCING PHASE DIFFERENCE
	12 11 10 9 8 7 6 5 3 2 1 3 2 1 3 2	#1	1	4 1
T=5	13 12 11 10 9 8 7 6 2 1 3 2 1 3 2 1	#3	3	3 1
	13 12 11 10 9 8 7 6 3 2 1 3 2 1 3 2	#2	2	6 1 START OF PHASE ADJUSTMENT, PHASE DIFFERENCE
	13 12 11 10 9 8 7 6 1 3 2 1 3 2 1 3	#1	1	5 2
T=6	14 13 12 11 10 9 8 7 3 2 1 3 2 1 3 2	#3	1=3-2	6 1 DISCARD CELL WHEN REDUCING PHASE DIFFERENCE
	14 13 12 11 10 9 8 7 1 3 2 1 3 2 1 3	#2	2	6 2
	14 13 12 11 10 9 8 7 2 1 3 2 1 3 2 1	#1	1	6 3 COMPLETION OF PHASE ADJUSTMENT

FIG.36

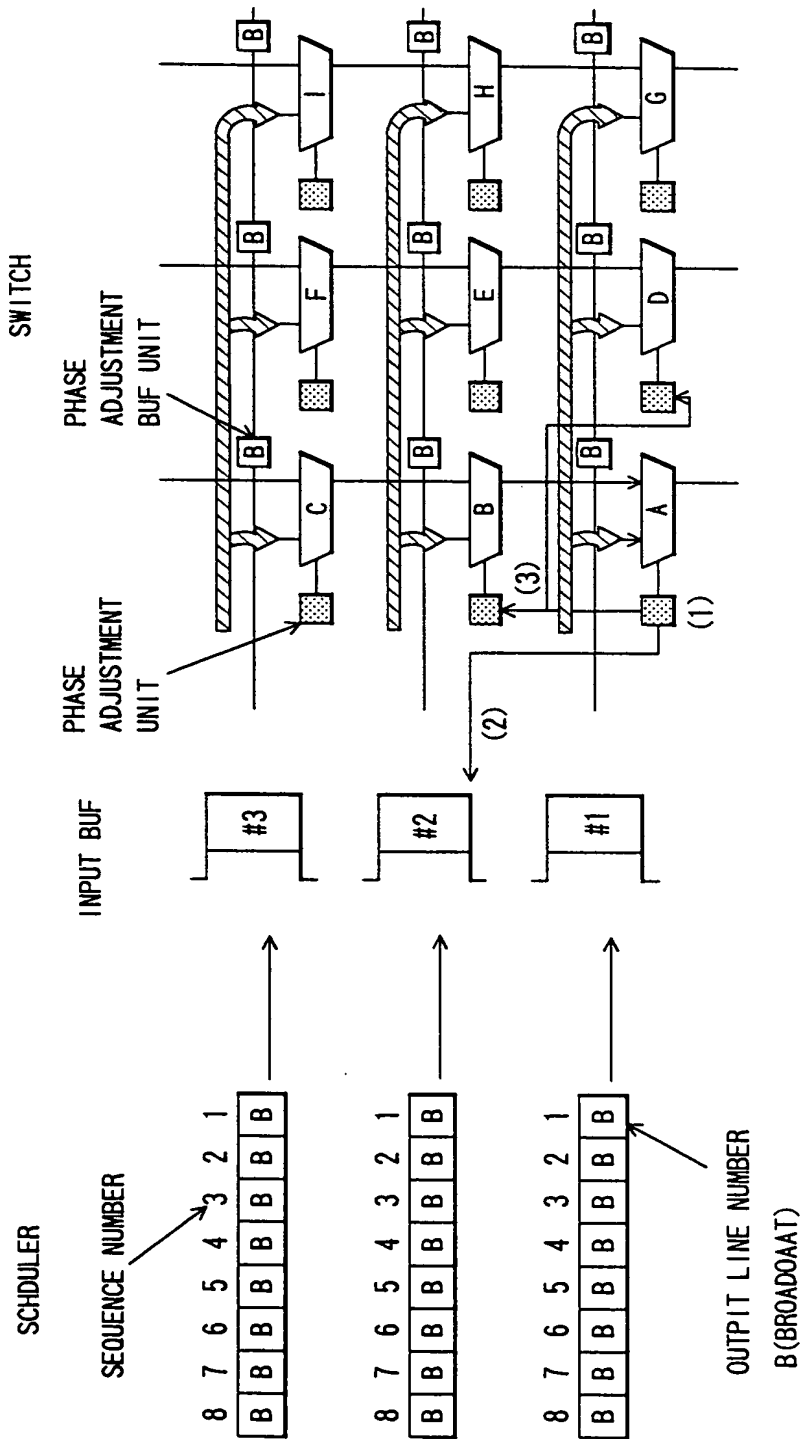


FIG.38

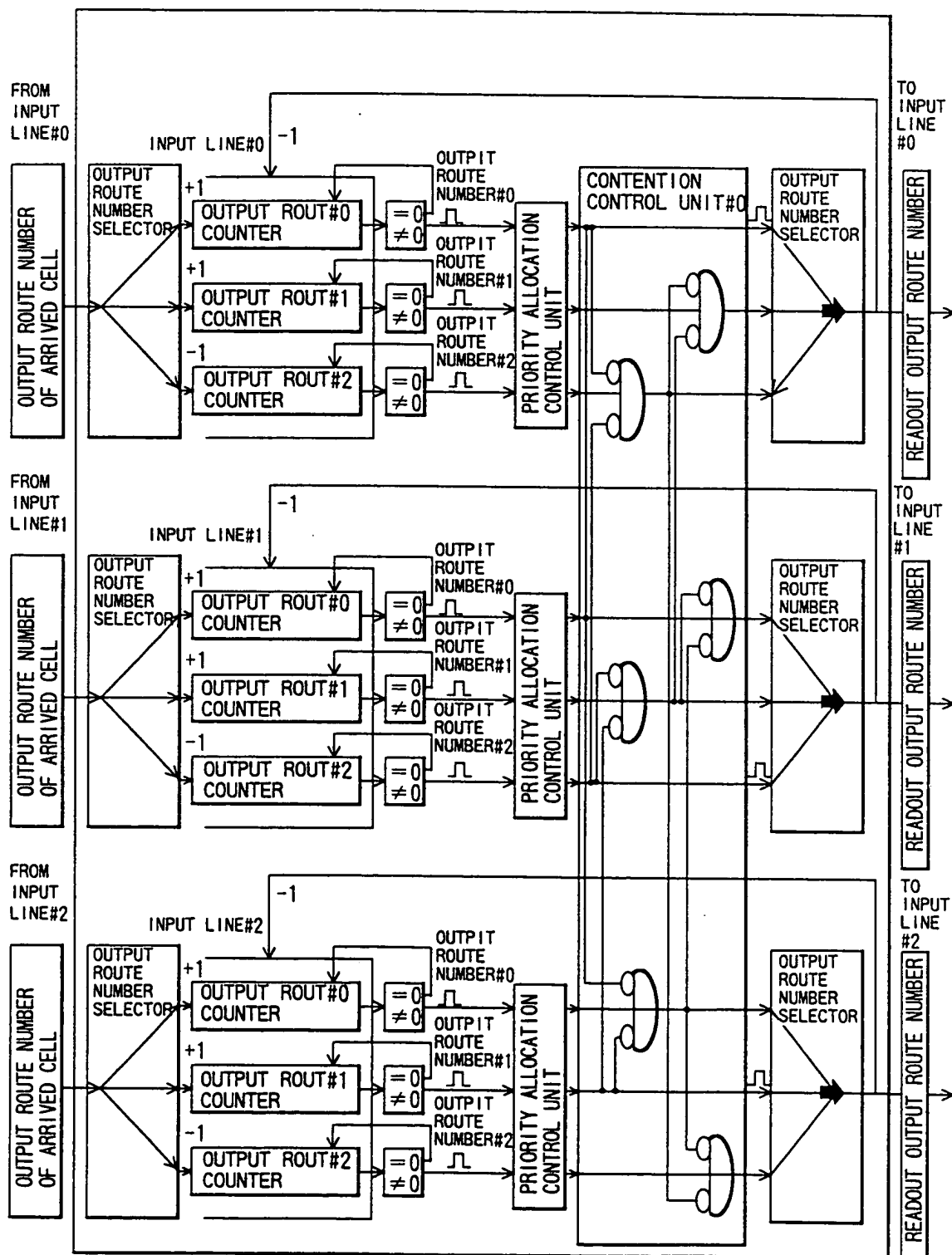


FIG.39

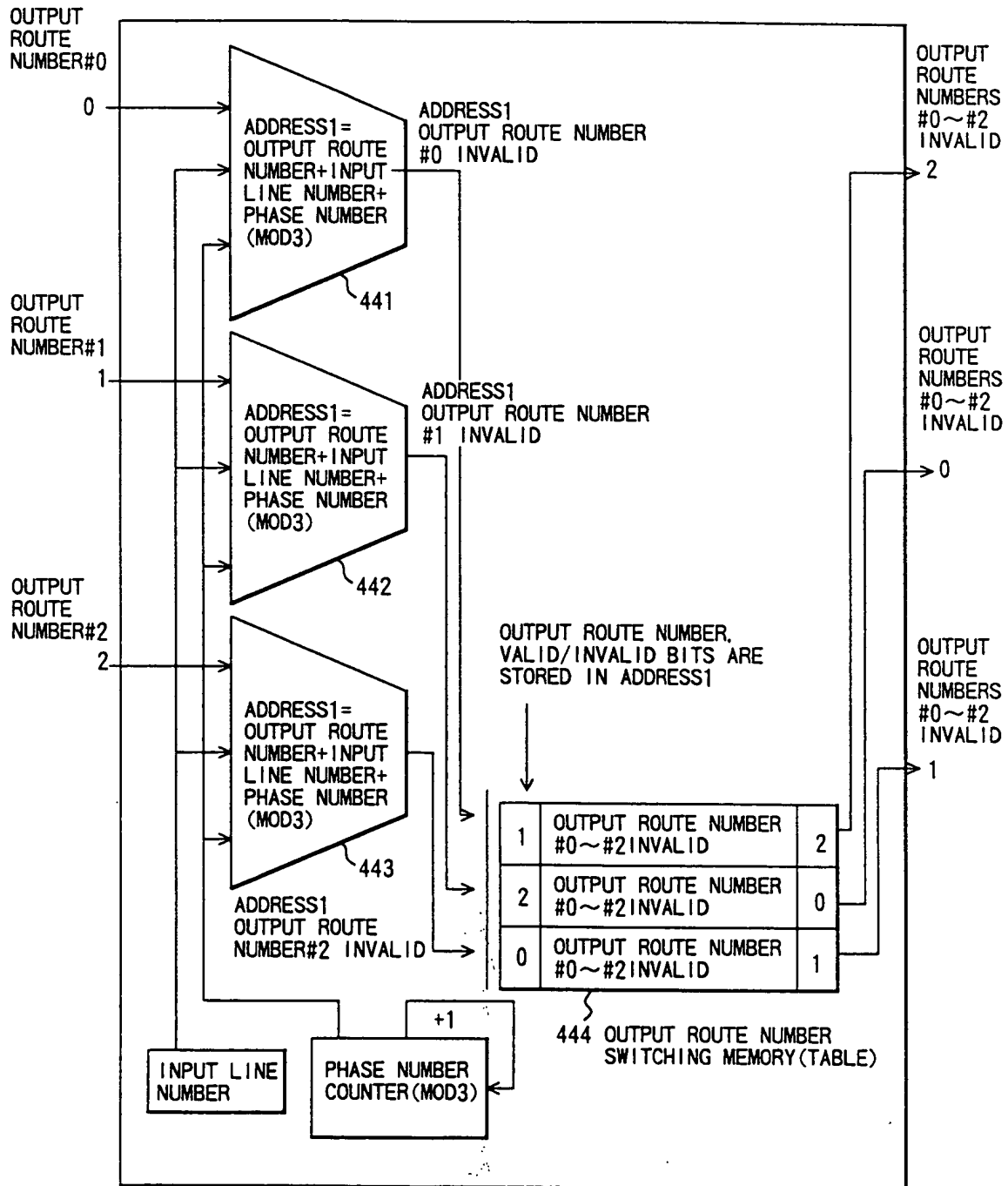


FIG.40

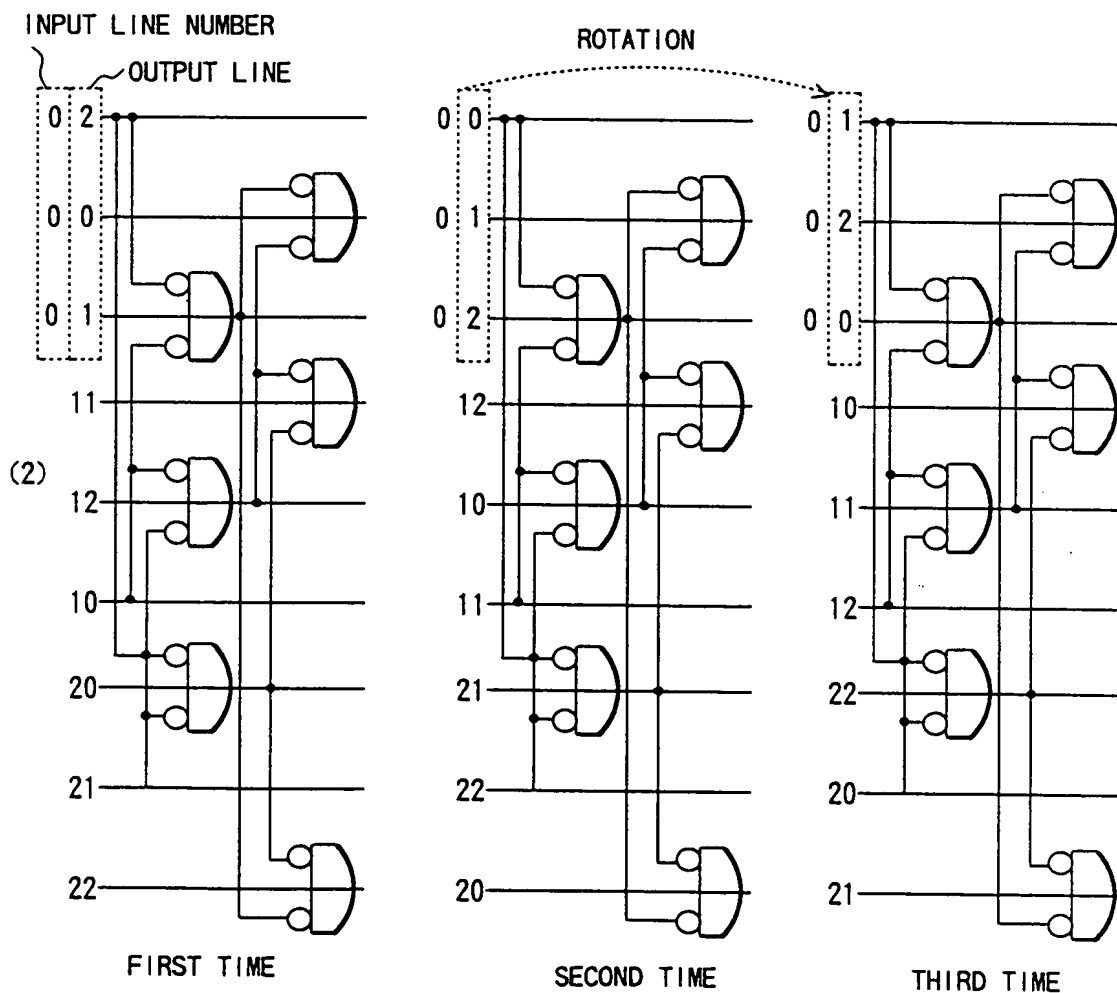
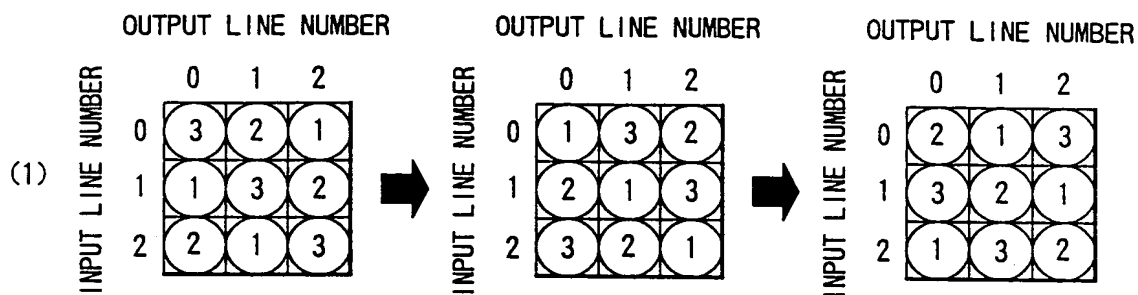


FIG.41

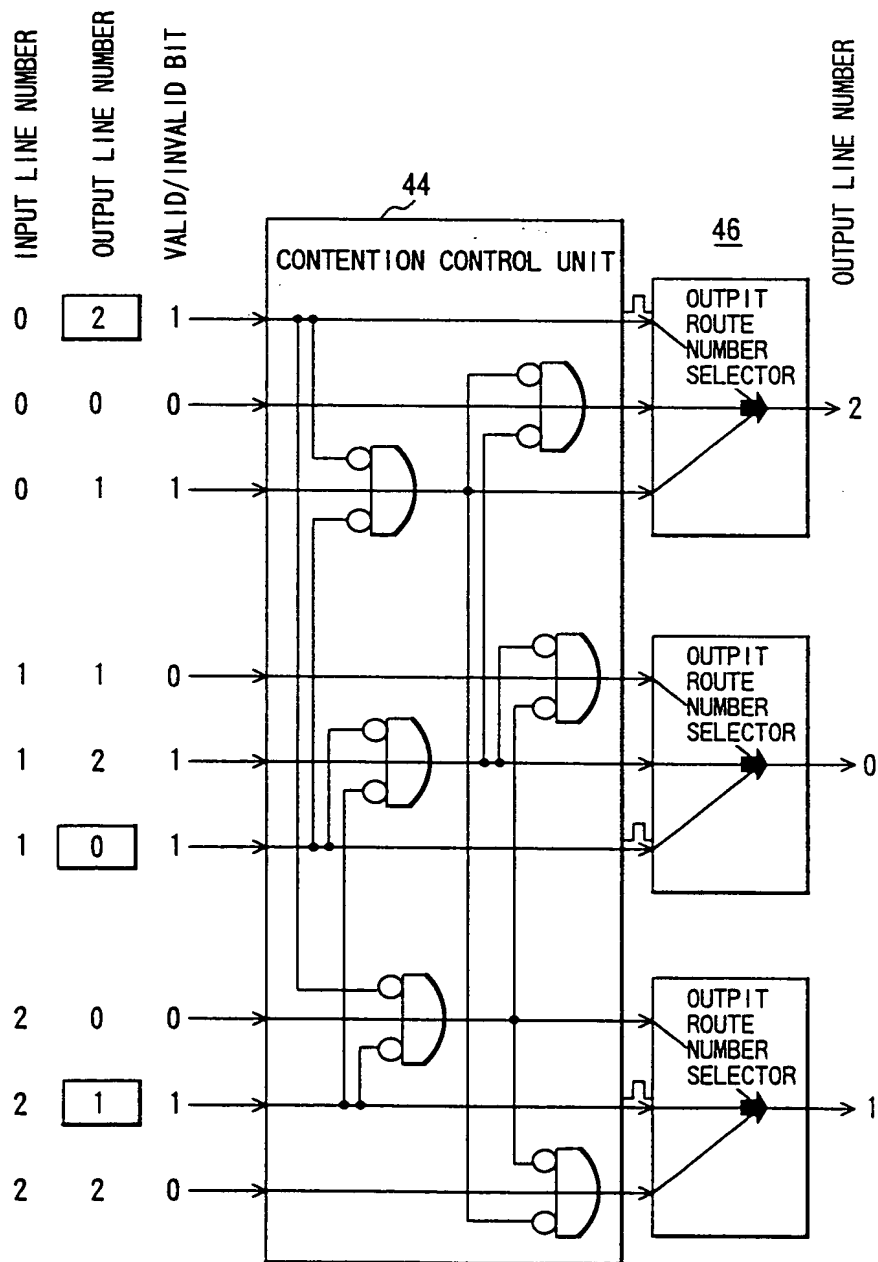
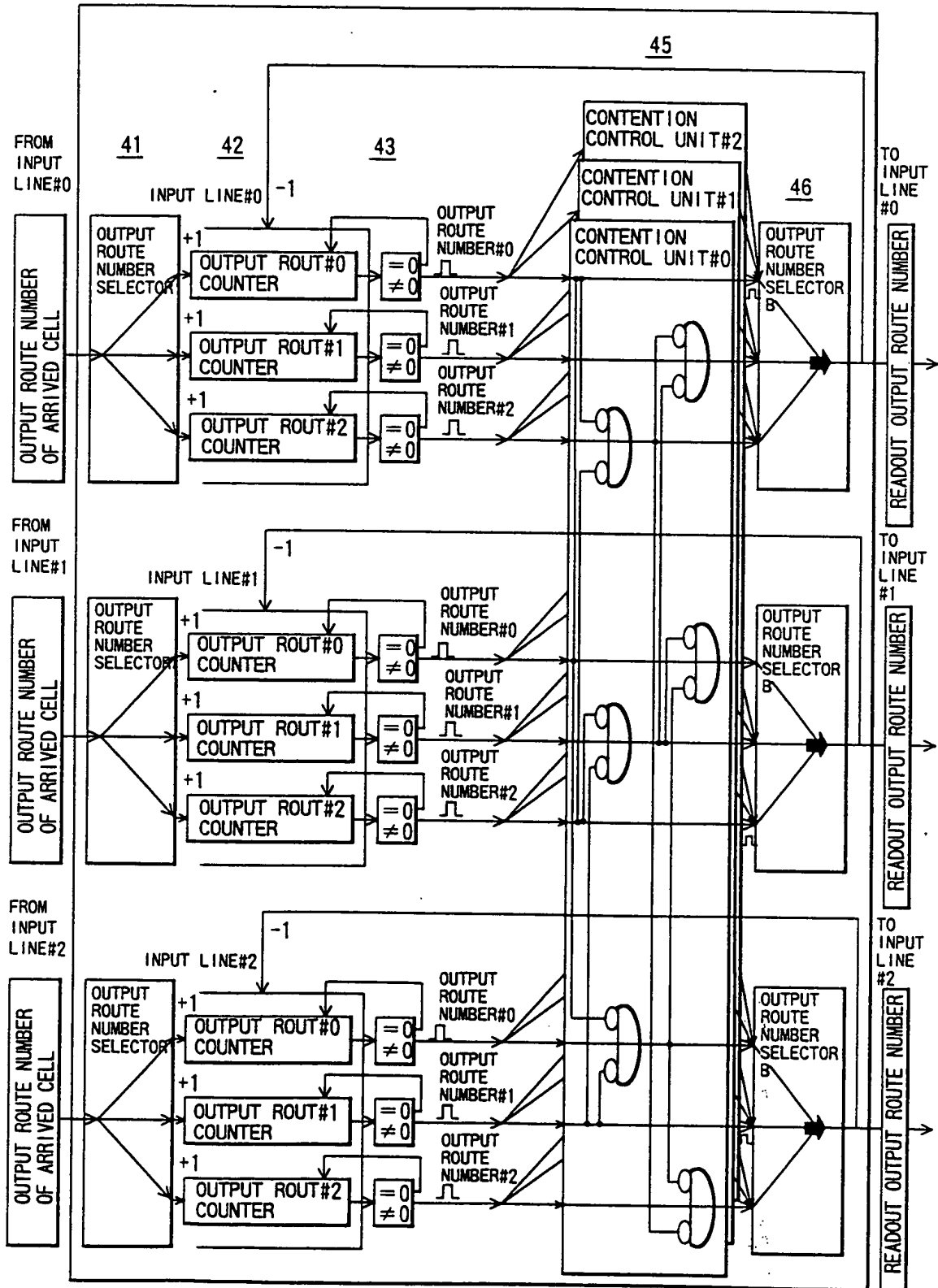


FIG.42



66472" 88809460

FIG. 43

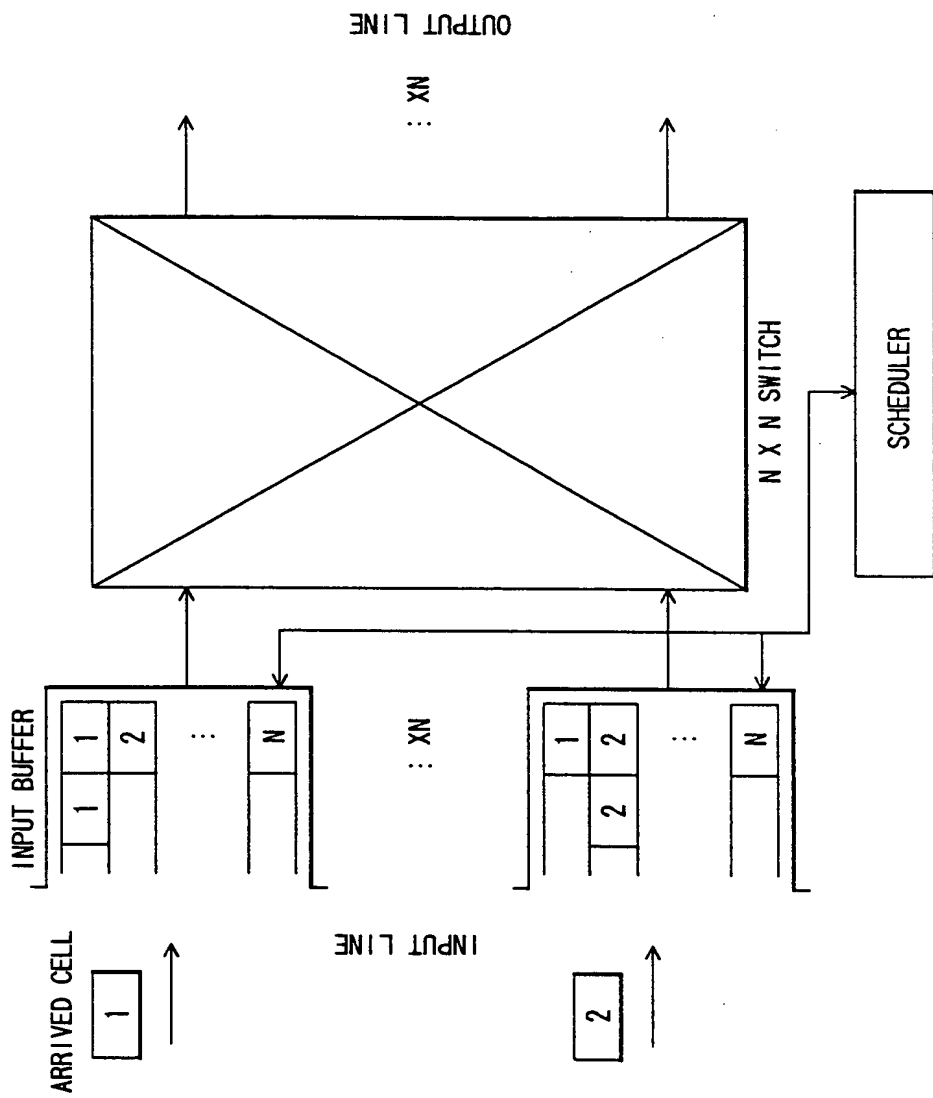
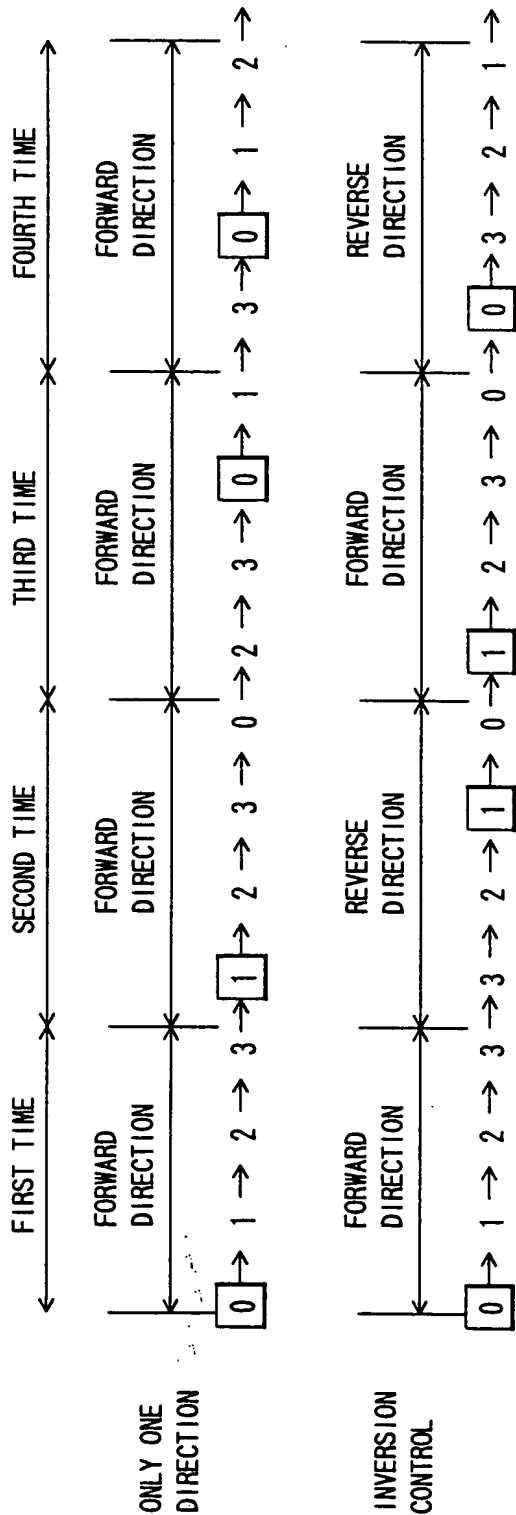


FIG.44



	ONE DIRECTION	INVERSION CONTROL
INPUT LINE #0 WITH TOP PRIORITY	3-TIMES/4-TIMES	TWICE/4-TIMES
INPUT LINE #1 WITH TOP PRIORITY	ONCE/4-TIMES	TWICE/4-TIMES

UNEQUAL → EQUAL

FIG.45

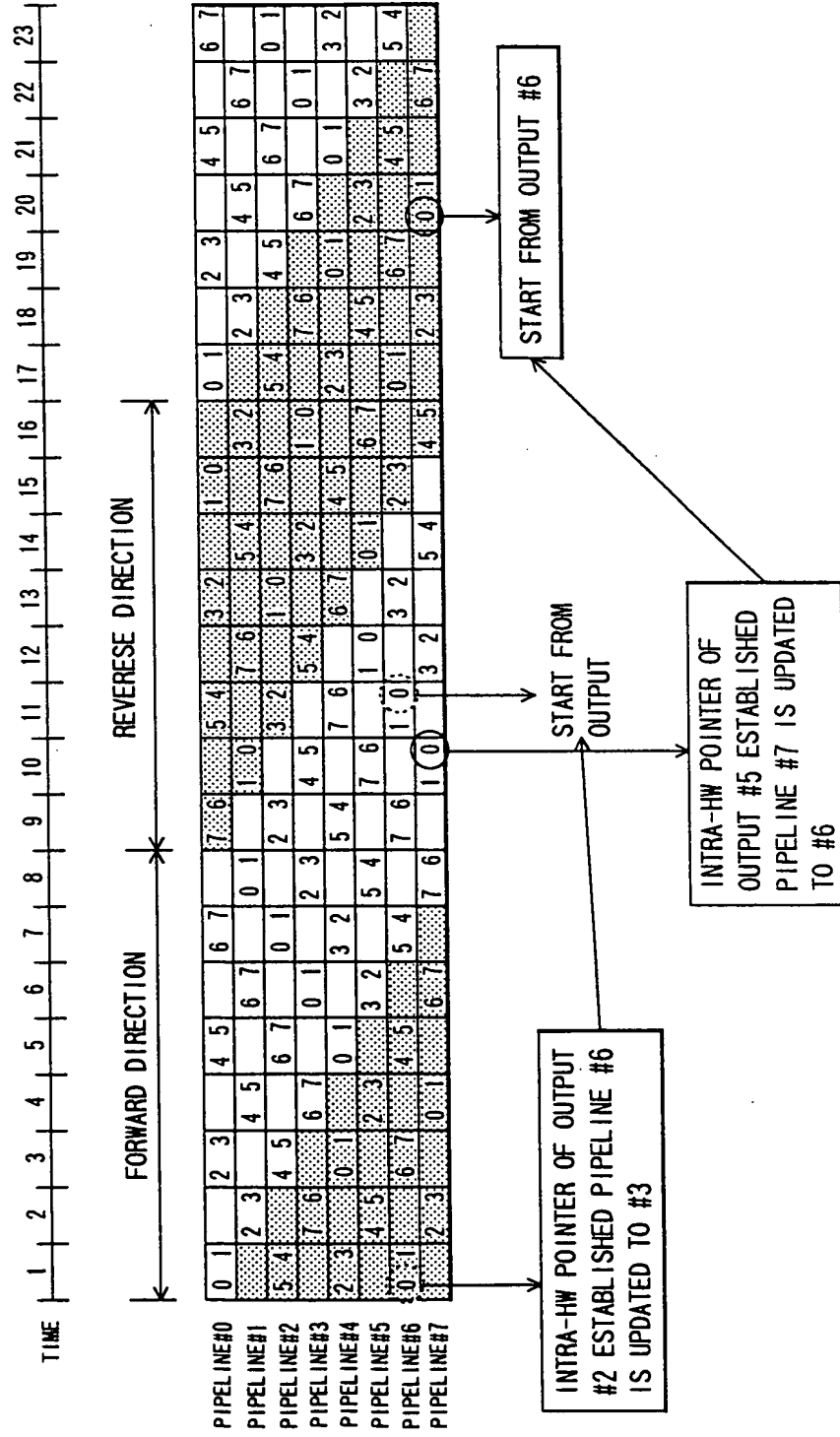


FIG.46

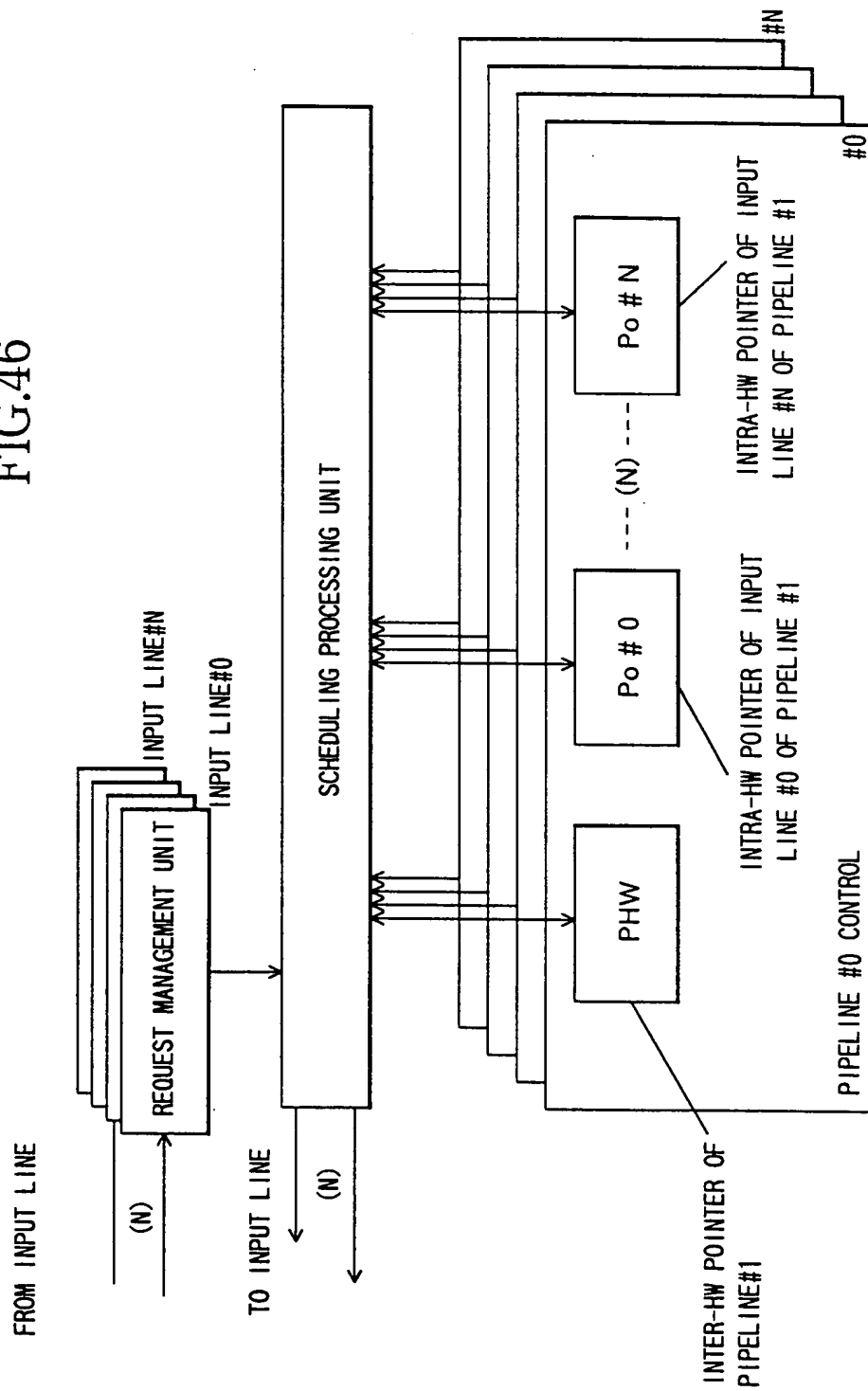


FIG.47

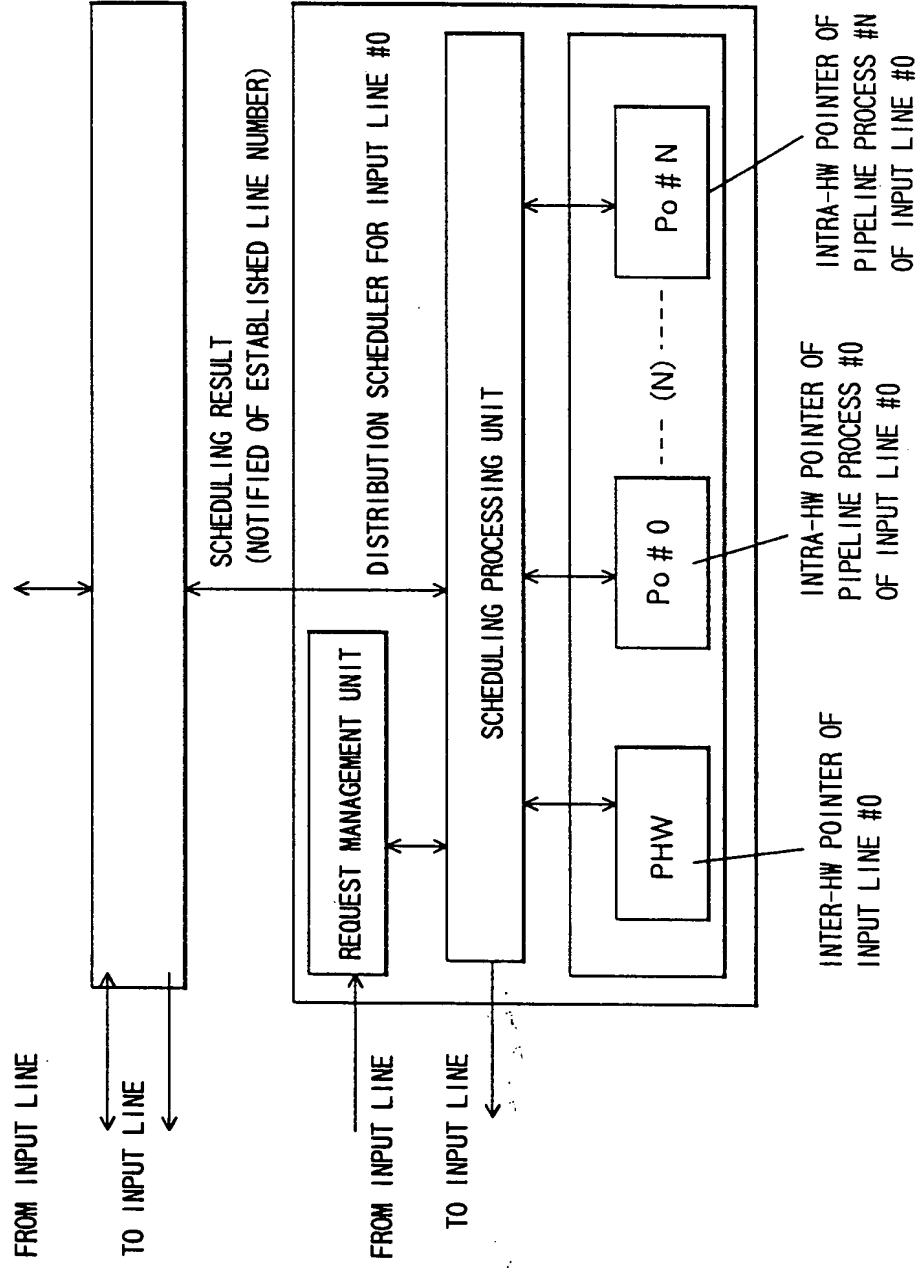
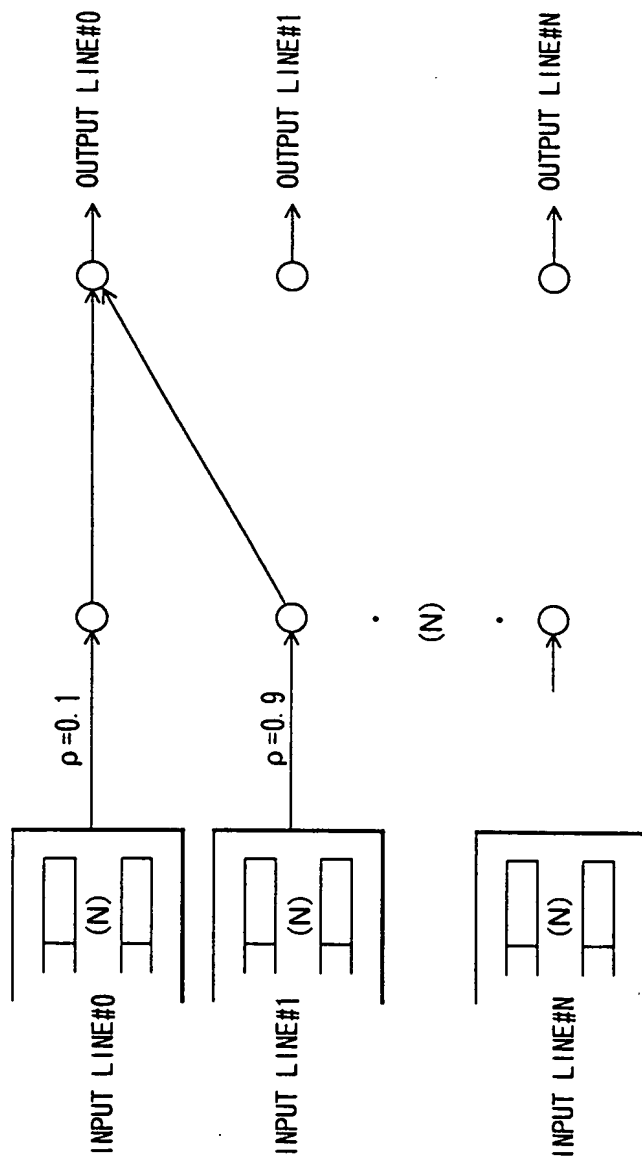


FIG.48



PATH: #0-#0 SELECTION PROBABILITY: 0.5 \rightarrow INPUT LOAD 0.1 \rightarrow NO PROBLEM

PATH: #1-#0 SELECTION PROBABILITY: 0.5 \rightarrow INPUT LOAD 0.9 \rightarrow INCREASED QUEUE LENGTH

FIG.49

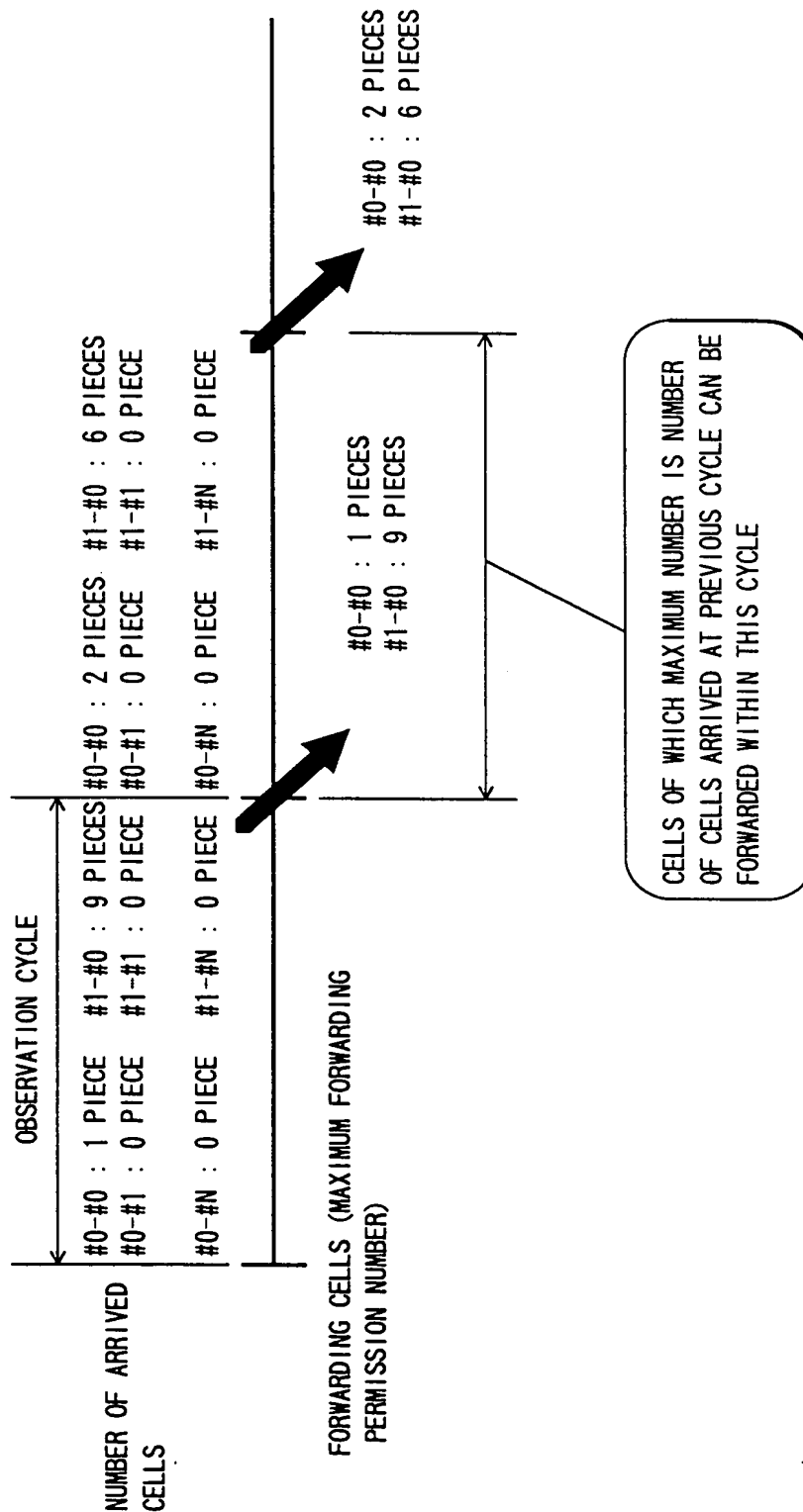


FIG. 50(a) LOAD OBSERVATION
FLOW

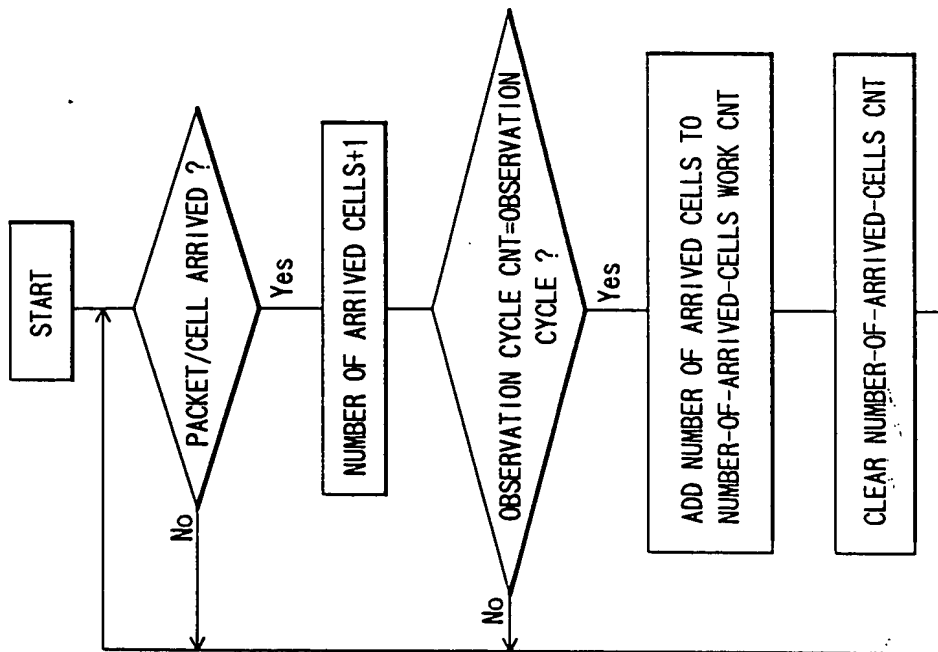


FIG. 50(b) SCHEDULING FLOW

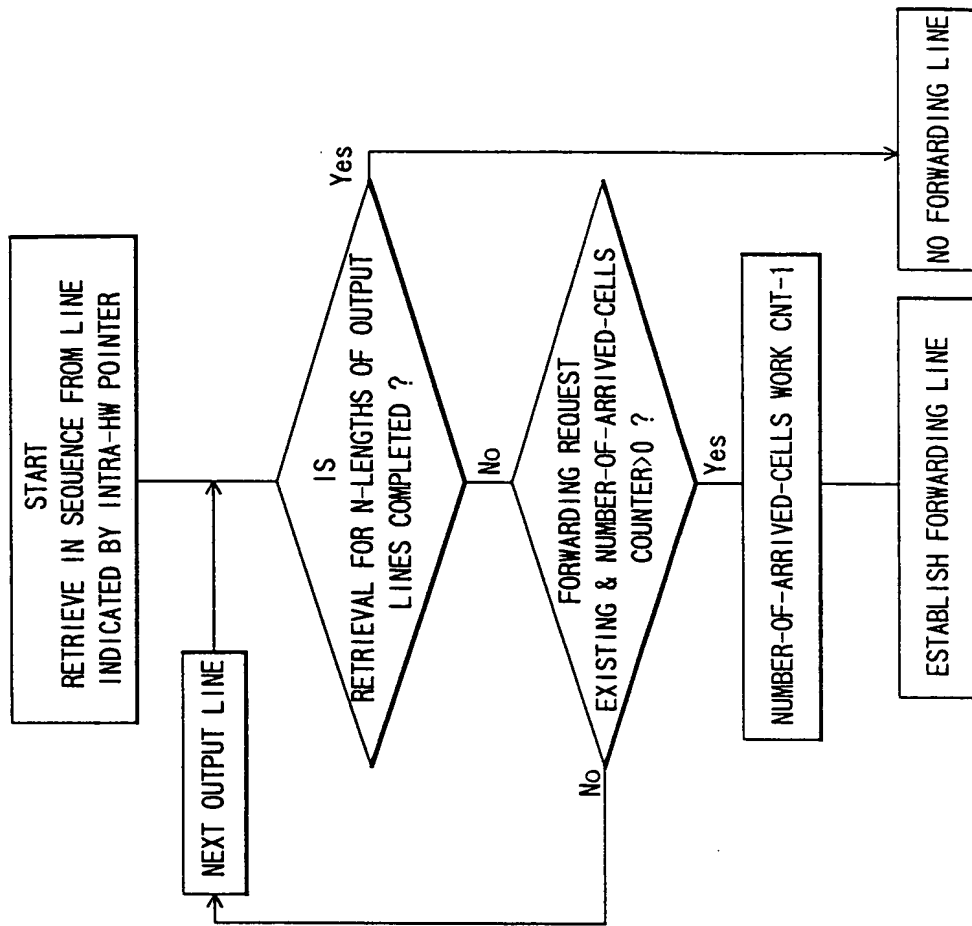


FIG.51

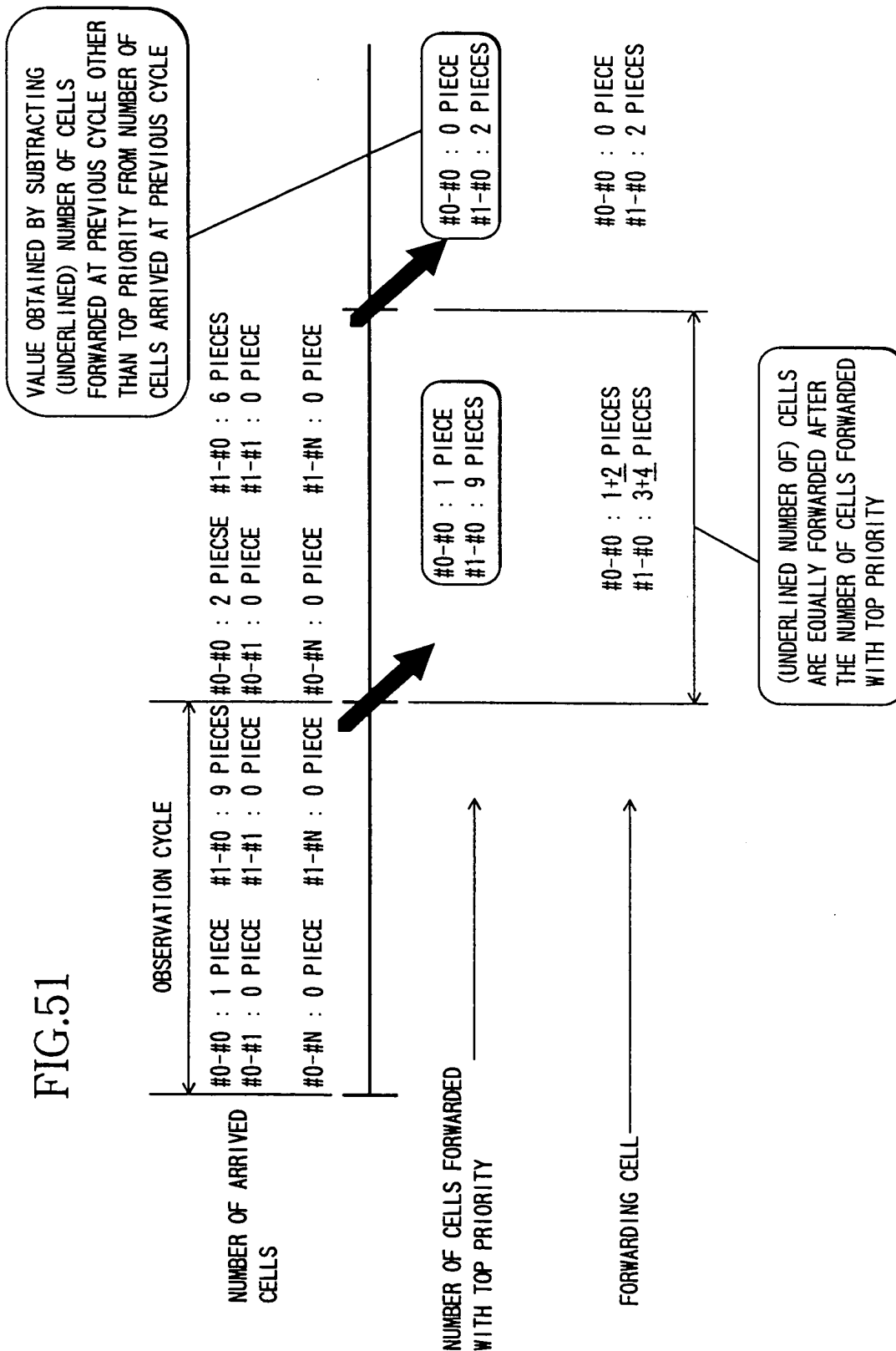


FIG52

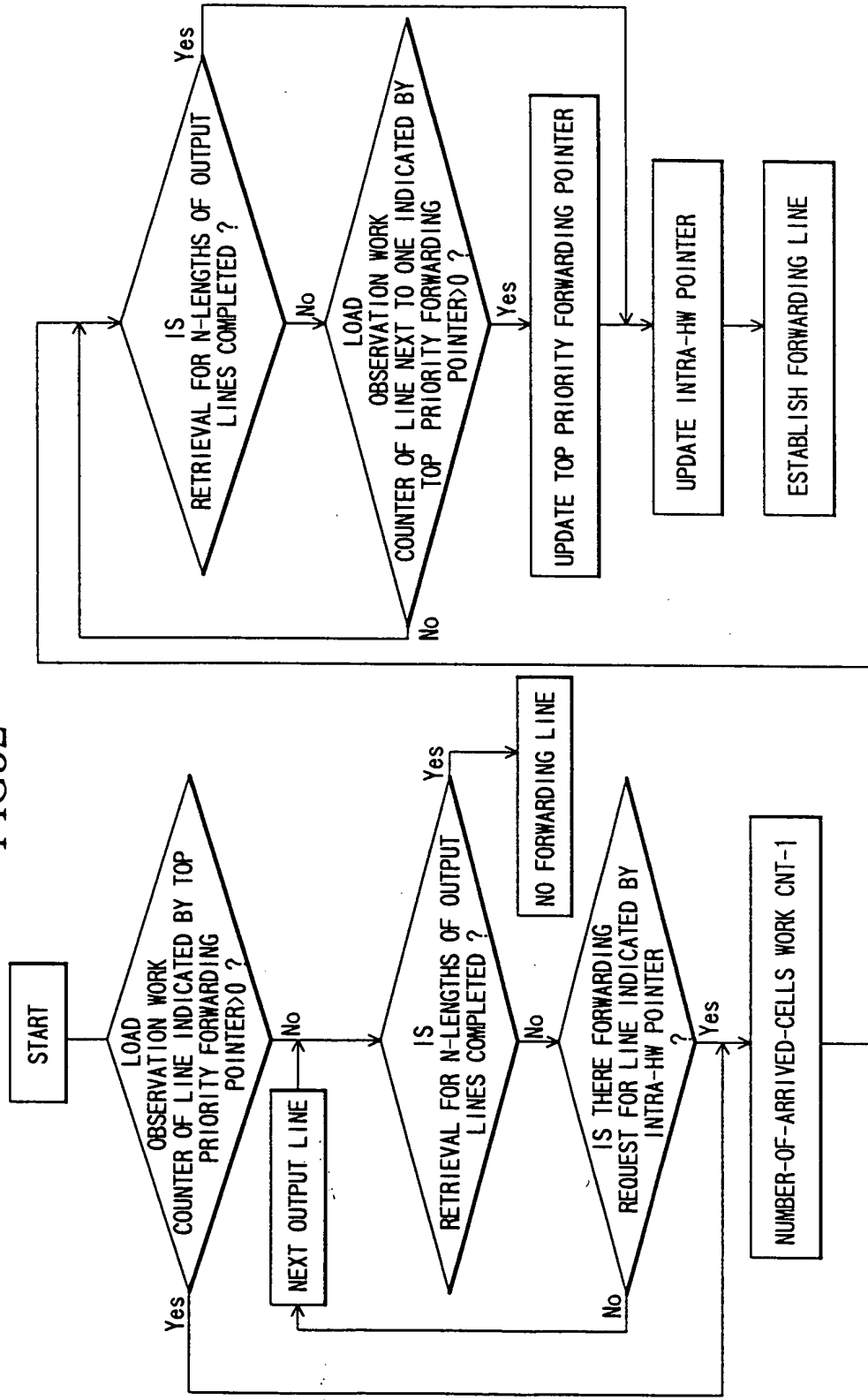


FIG.53

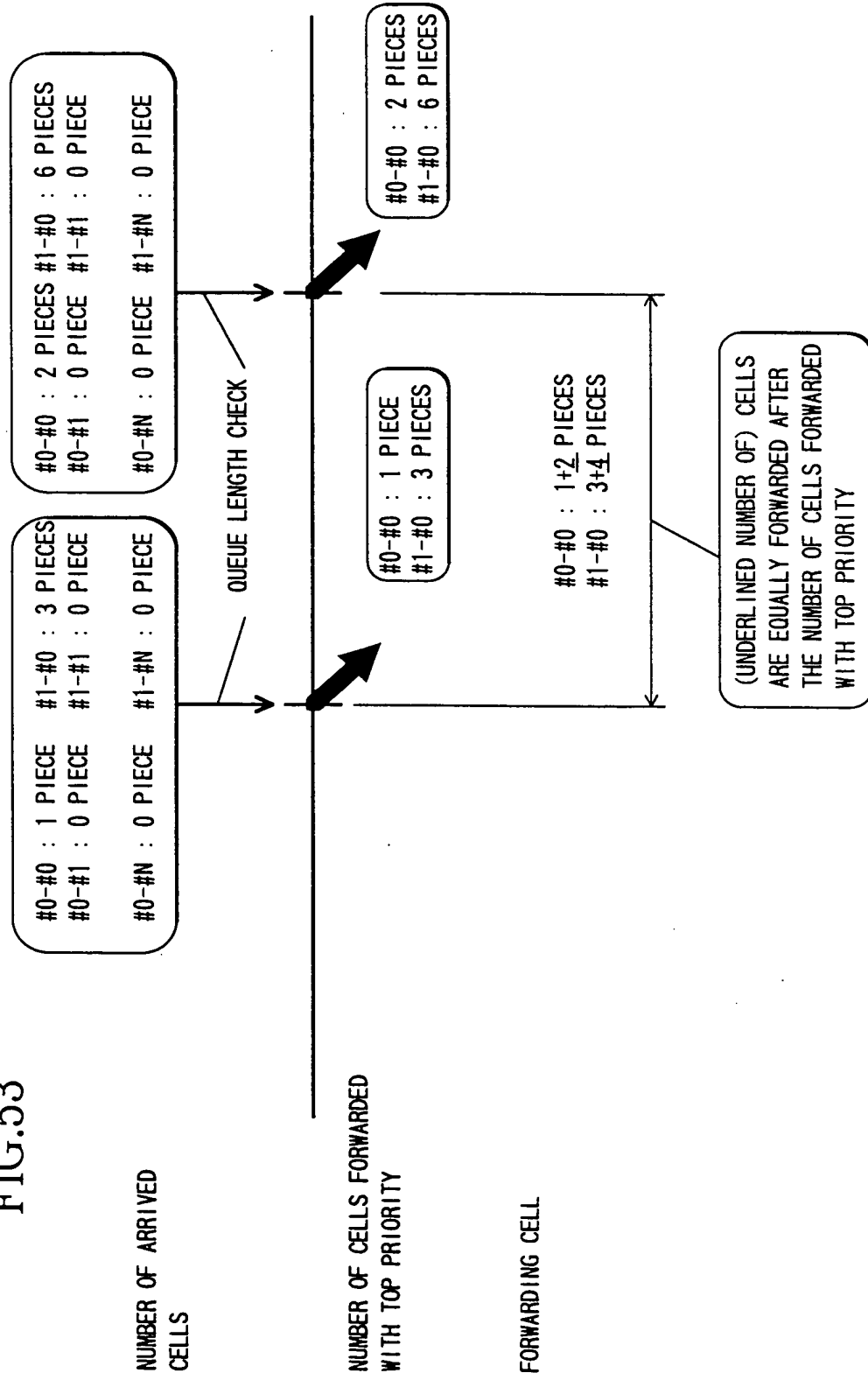


FIG. 54(a) LOAD OBSERVATION FLOW ON
QUEUE LENGTH BASE (PART 1)

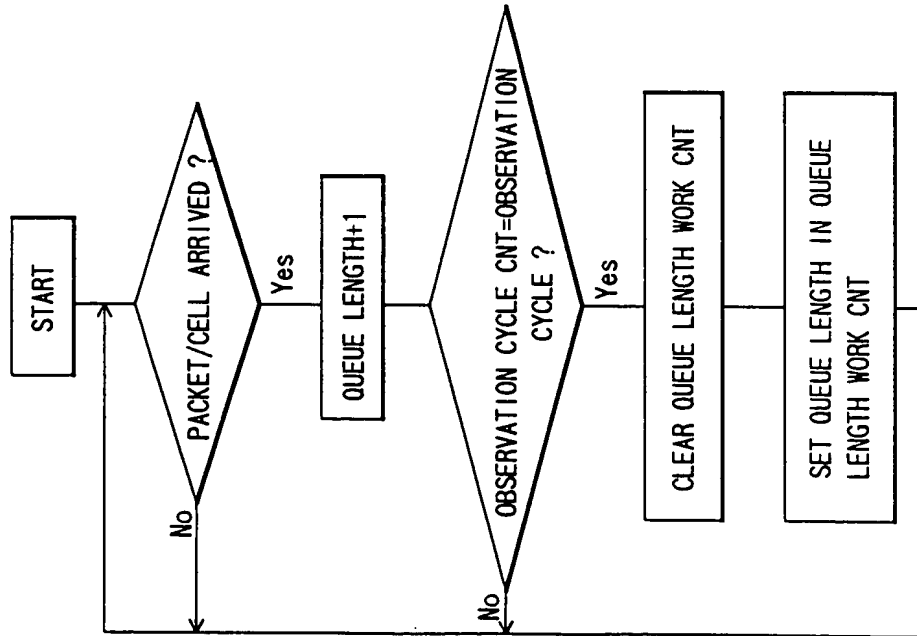


FIG. 54(b)(c) LOAD OBSERVATION FLOW
BASED ON QUEUE LENGTH BASE (PART 2)

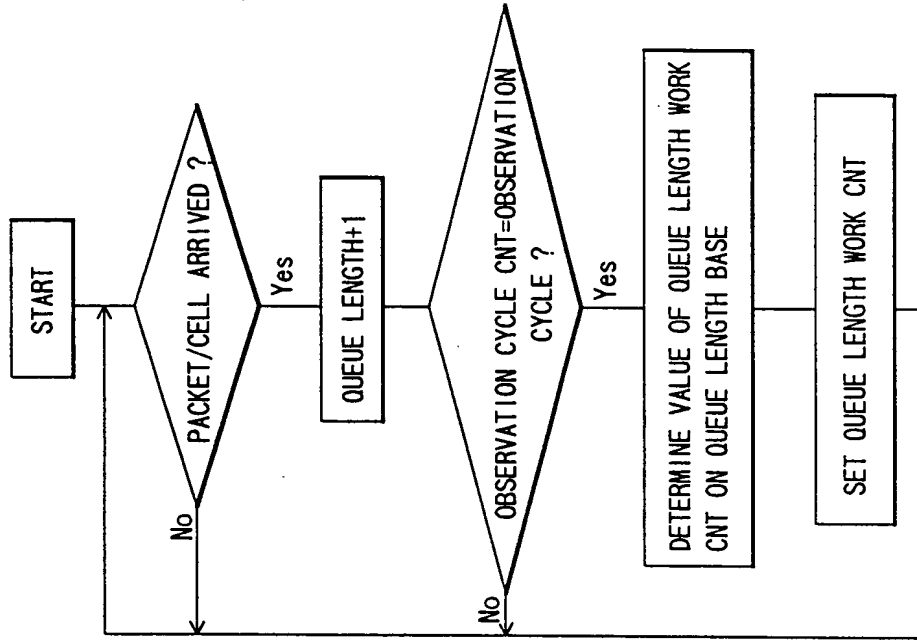
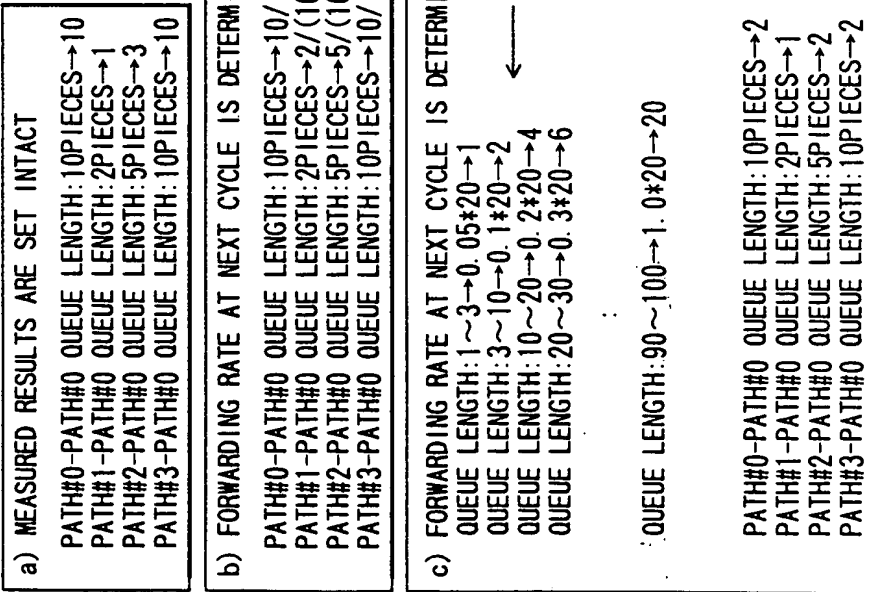


FIG.55



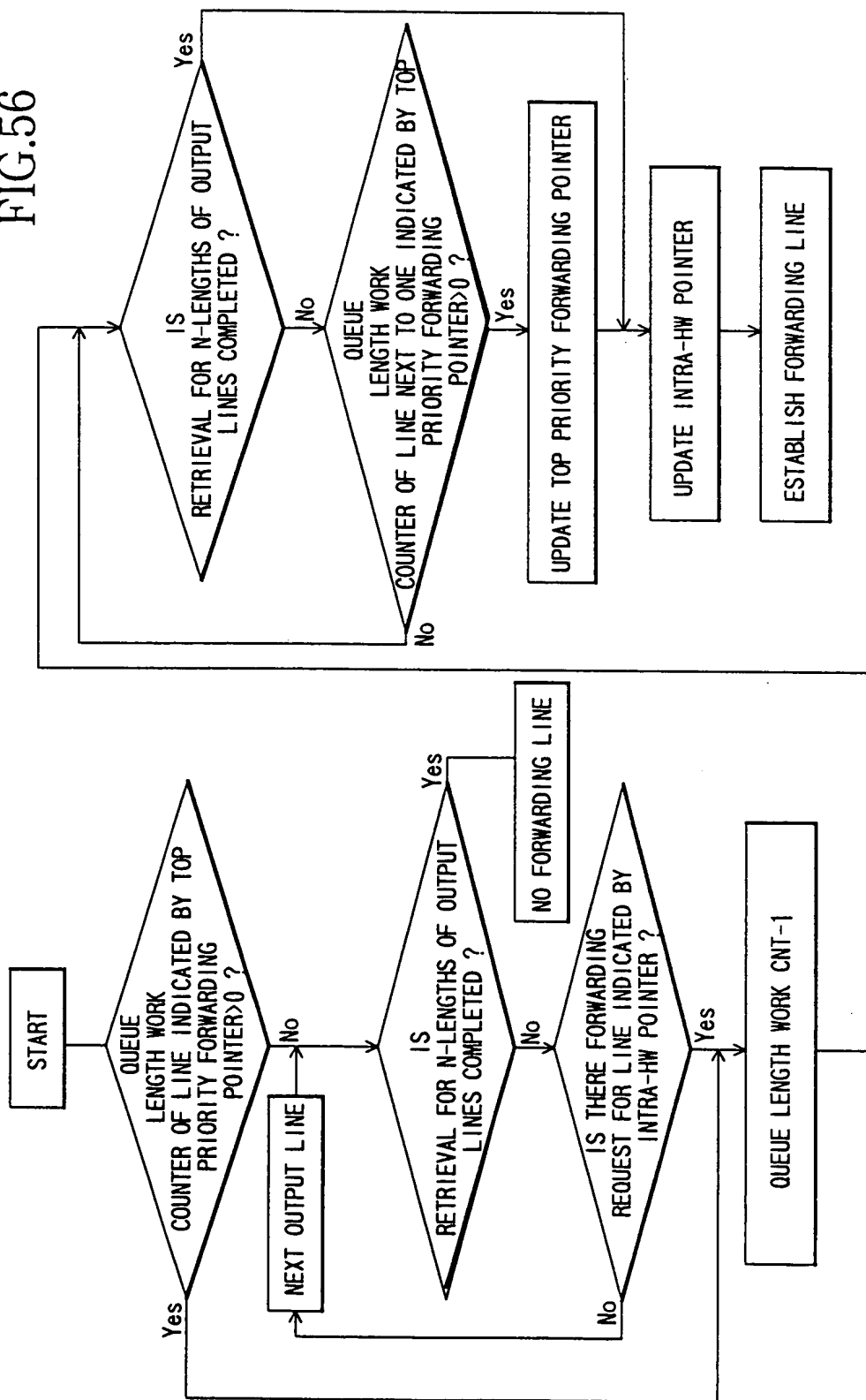


FIG.57

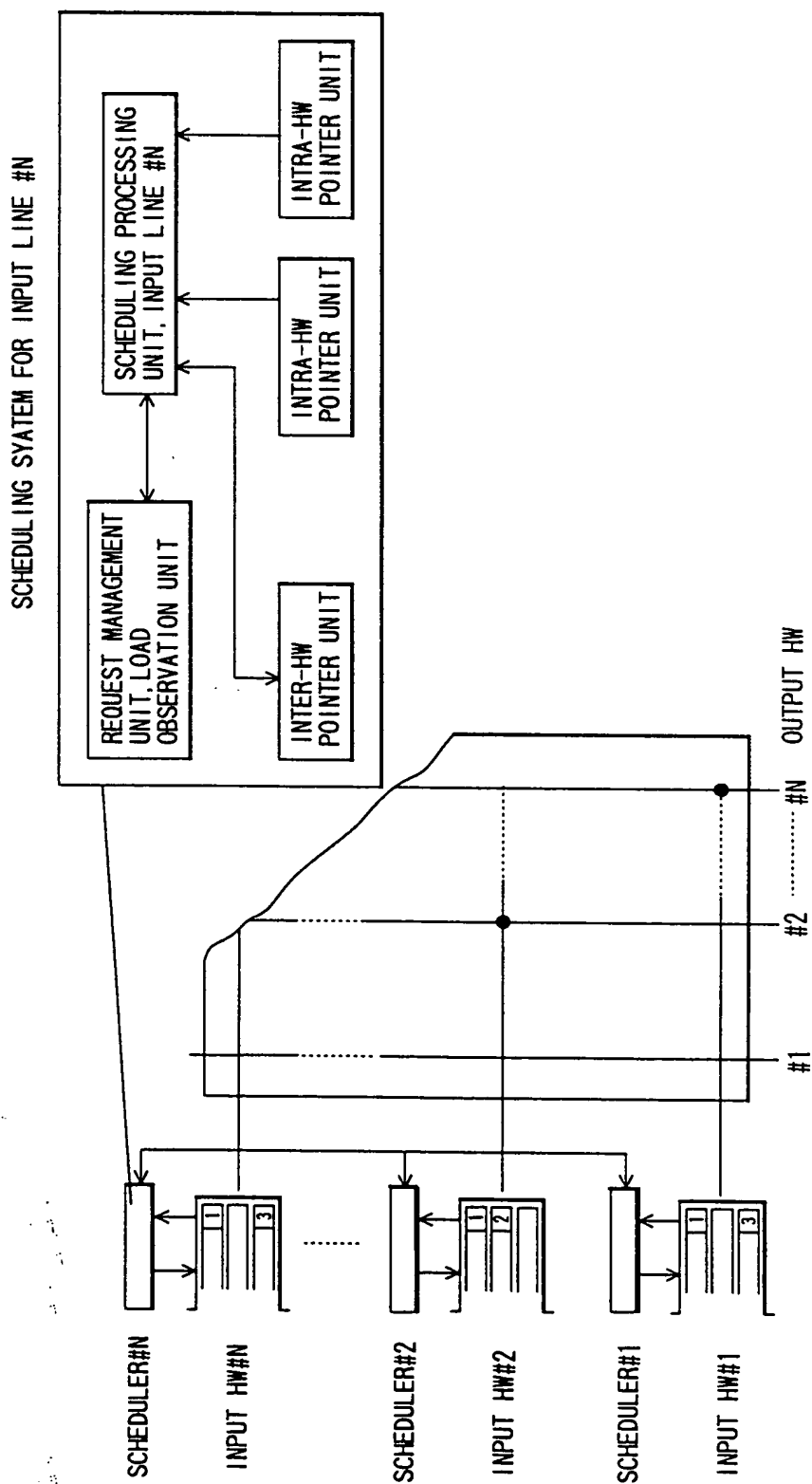


FIG. 58(a)RING CONNECTION

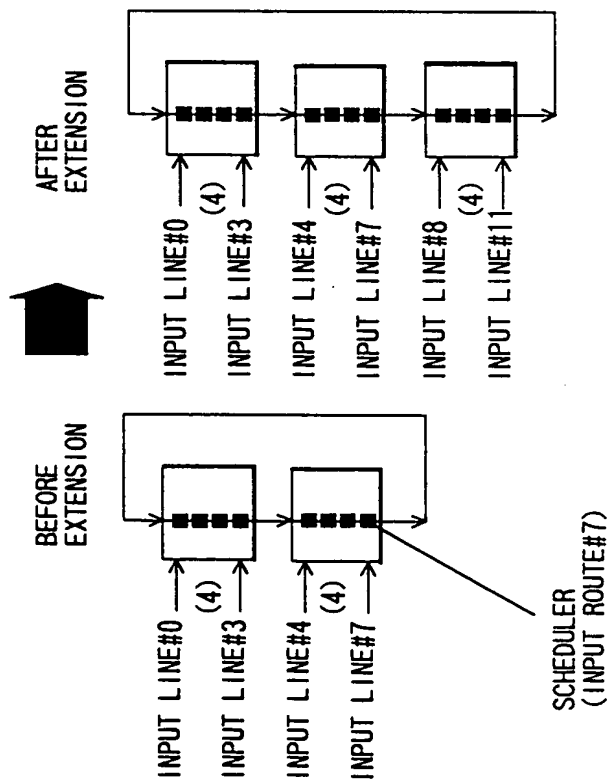


FIG. 58(b)TANDEM CONNECTION

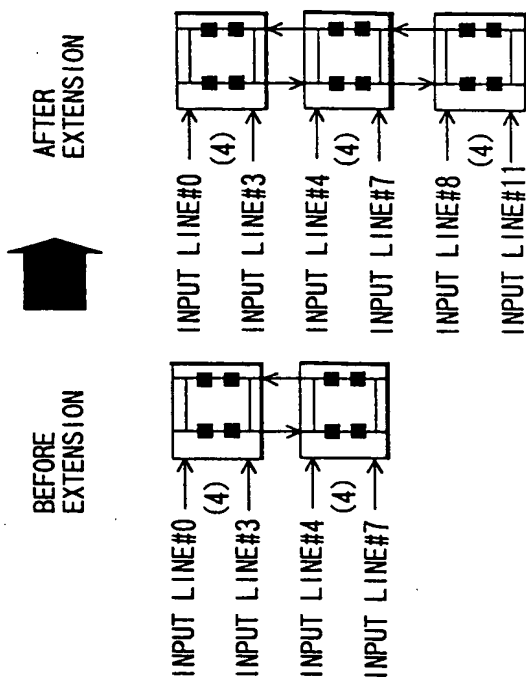


FIG. 59

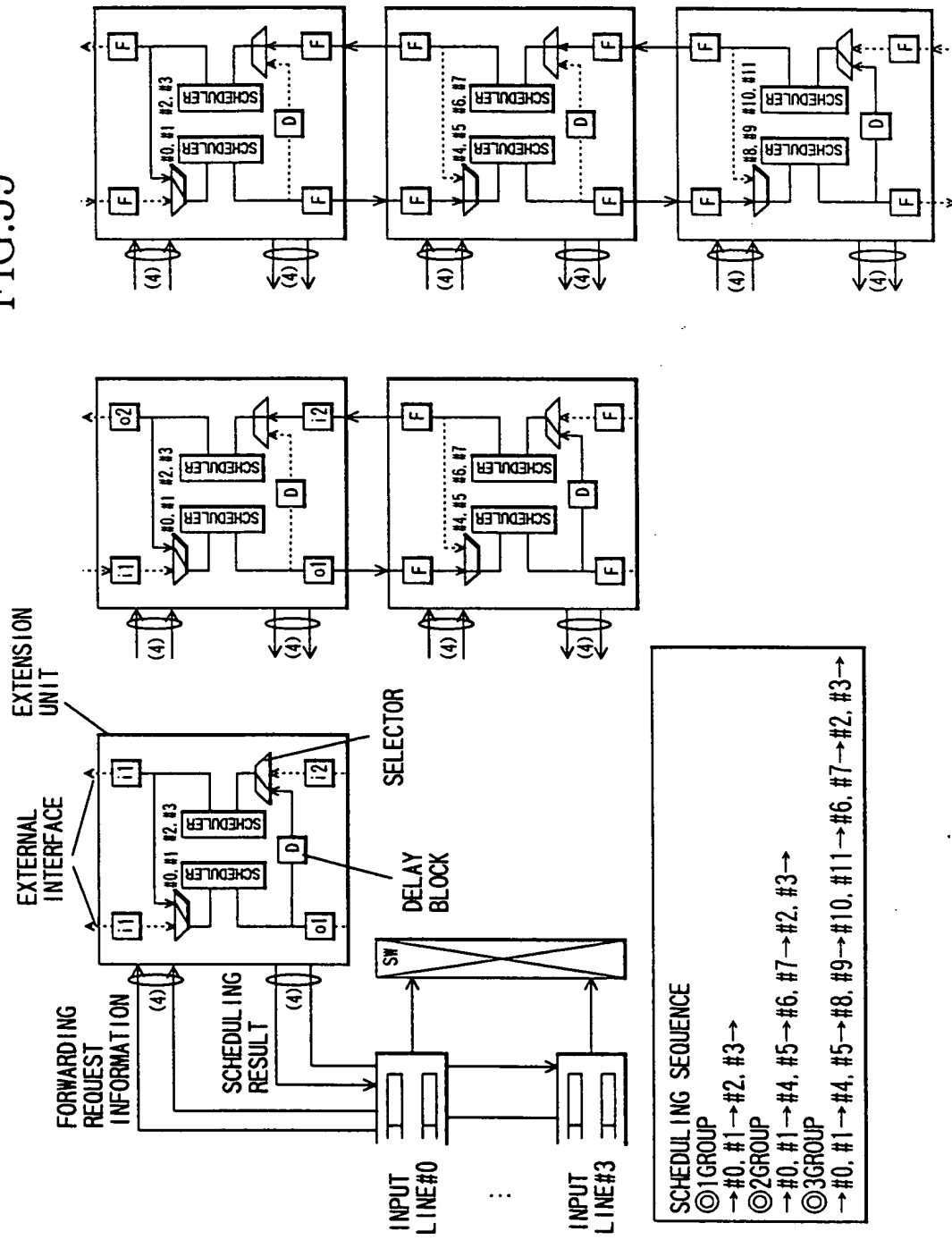


FIG. 60

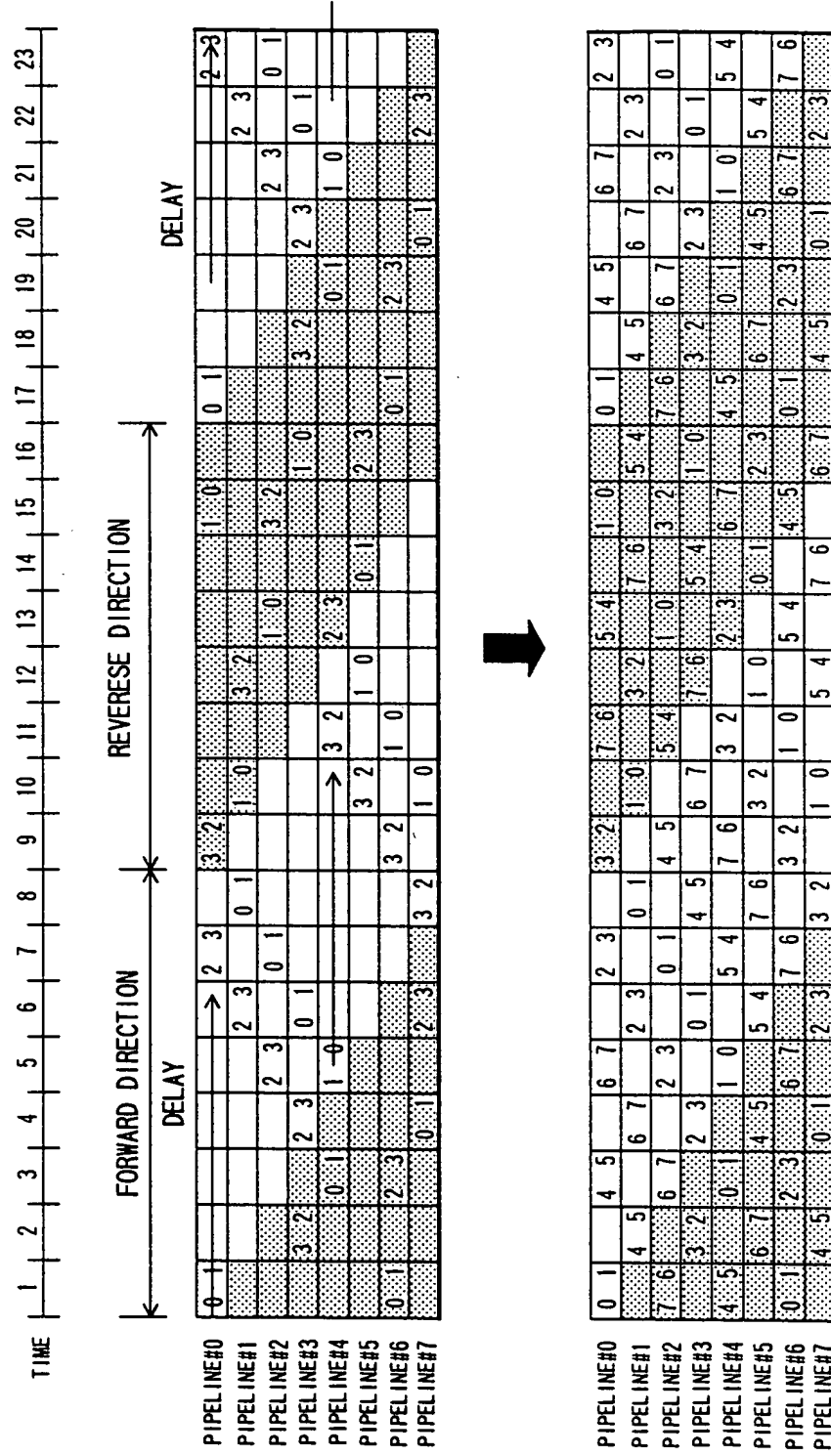


FIG. 61

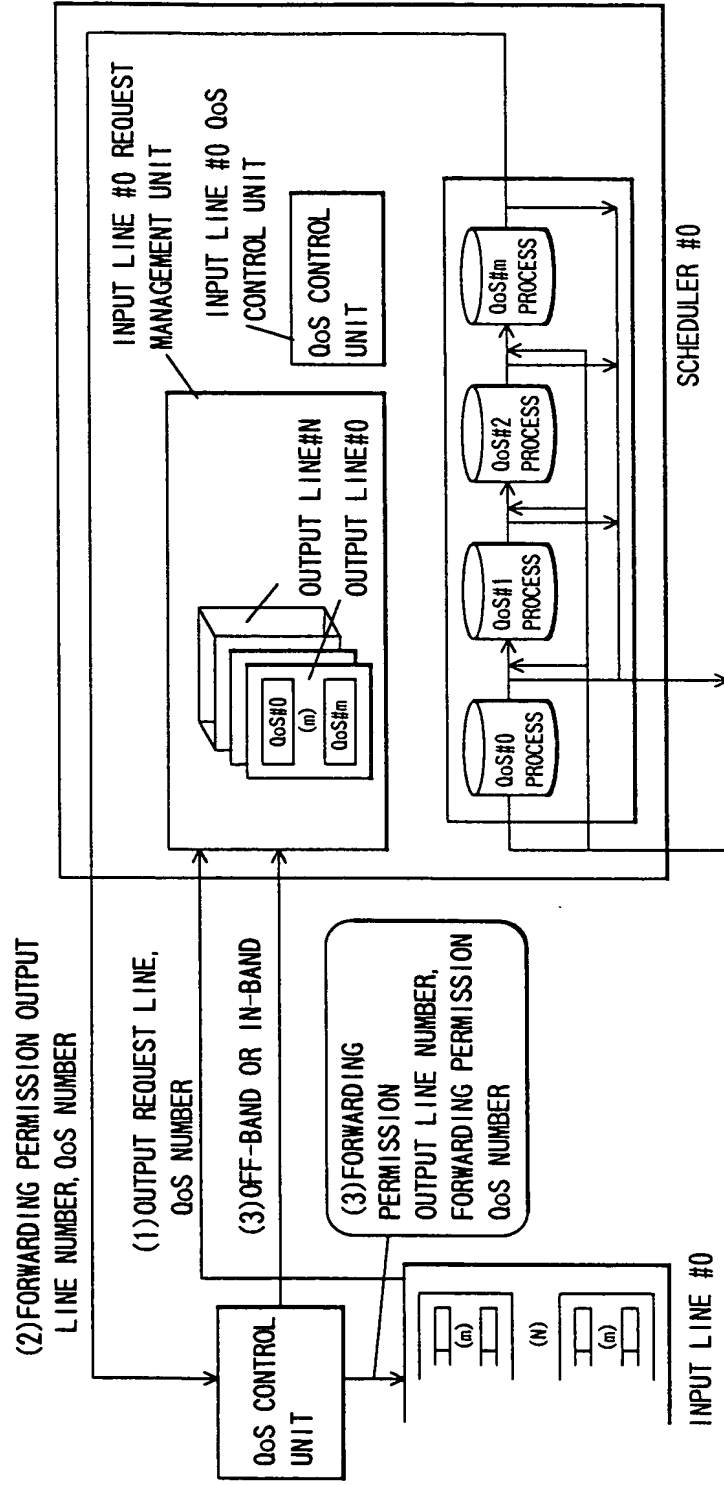
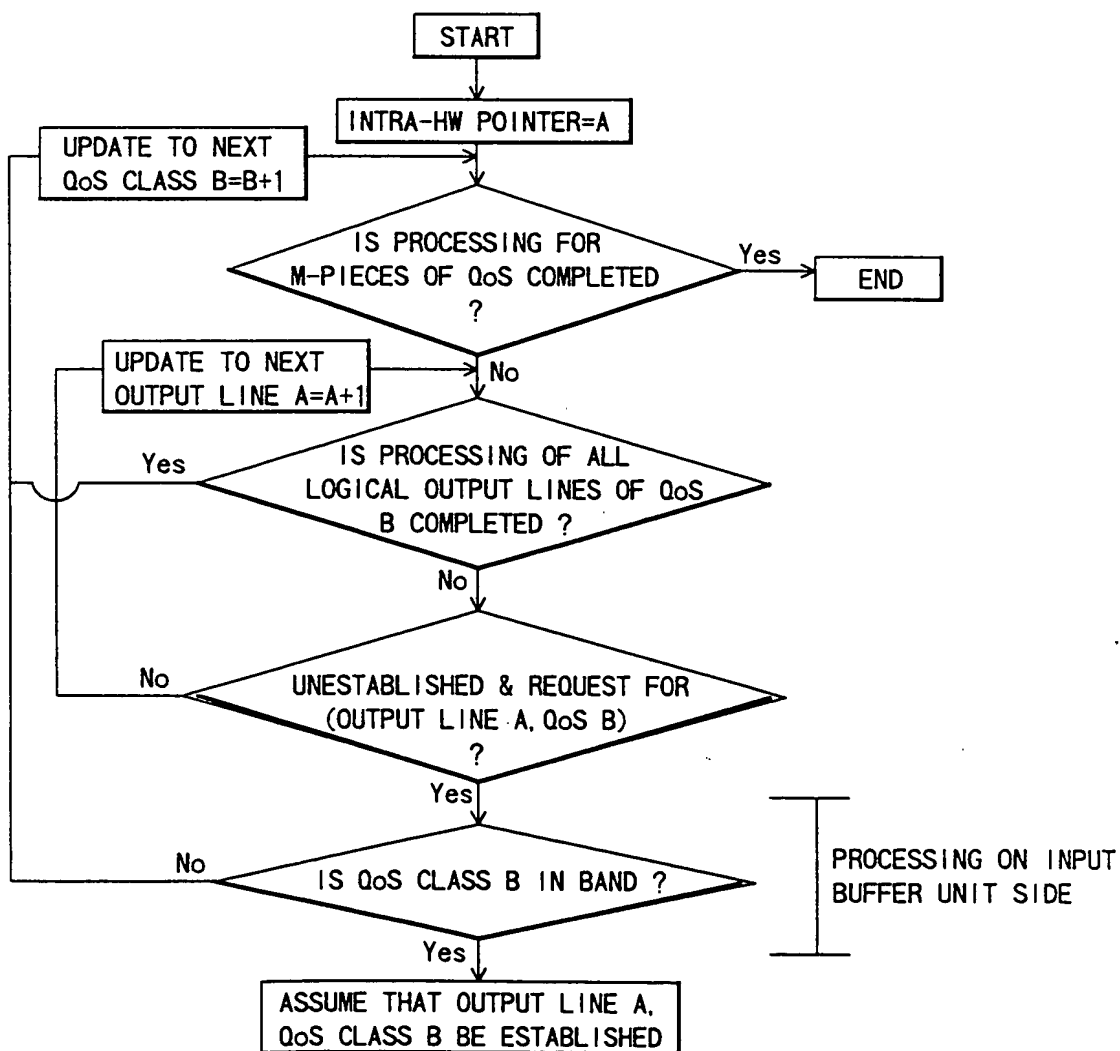


FIG.62



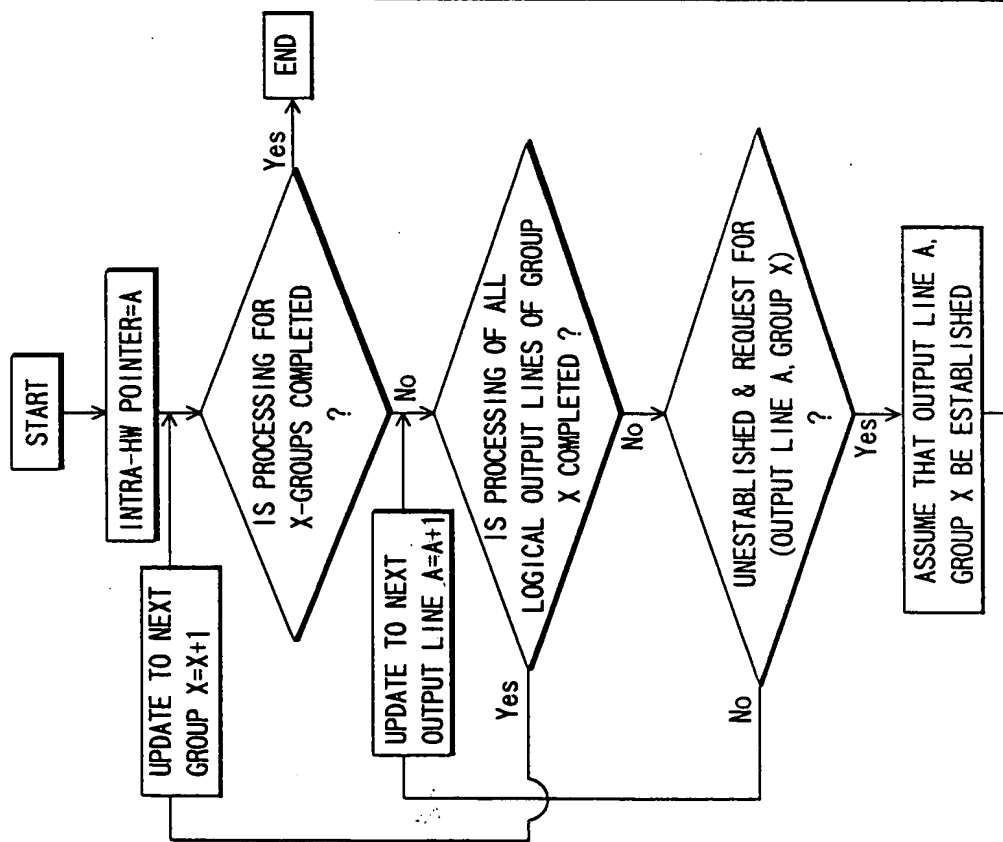
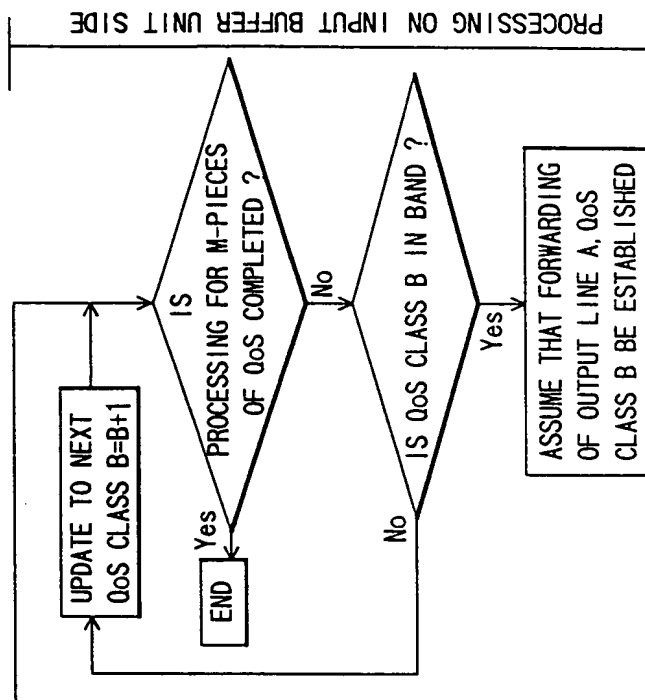


FIG.63



PROCESSING ON INPUT BUFFER UNIT SIDE

FIG.64

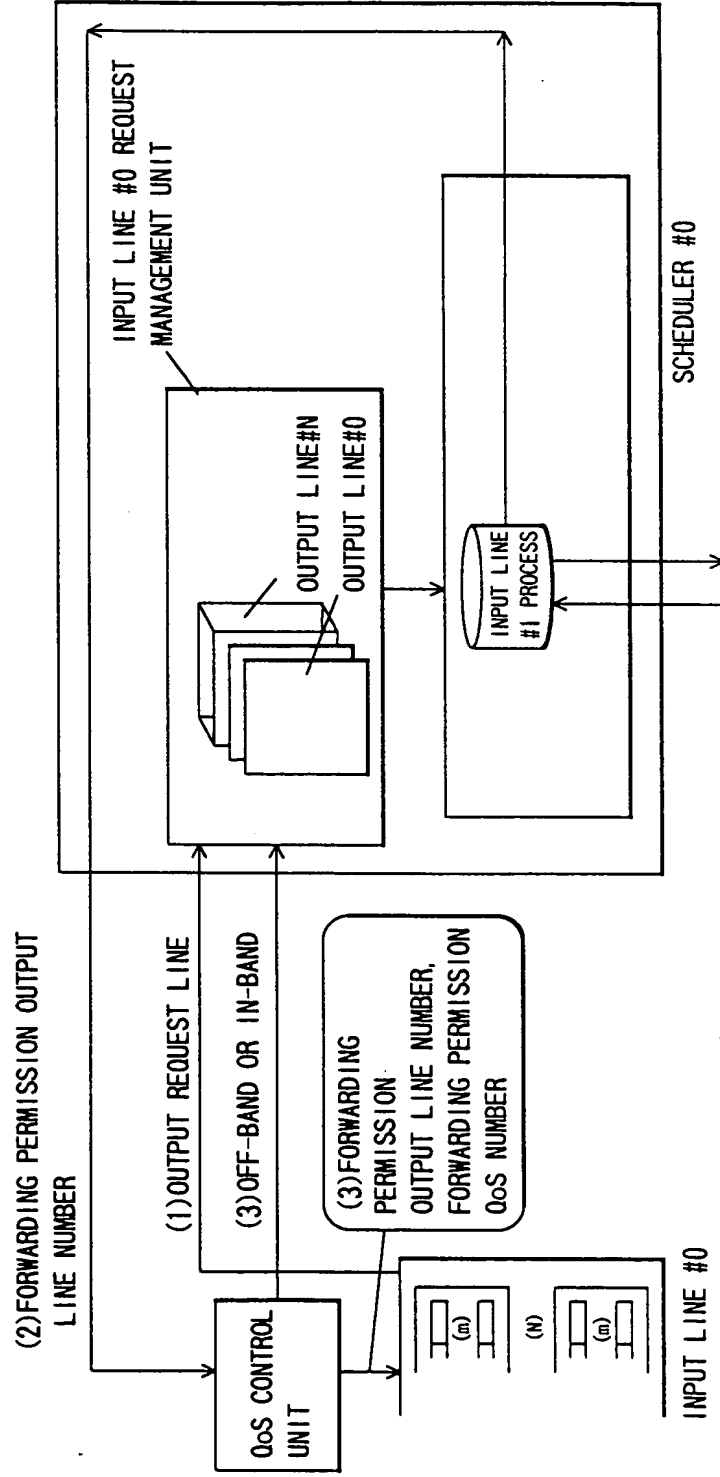


FIG.65

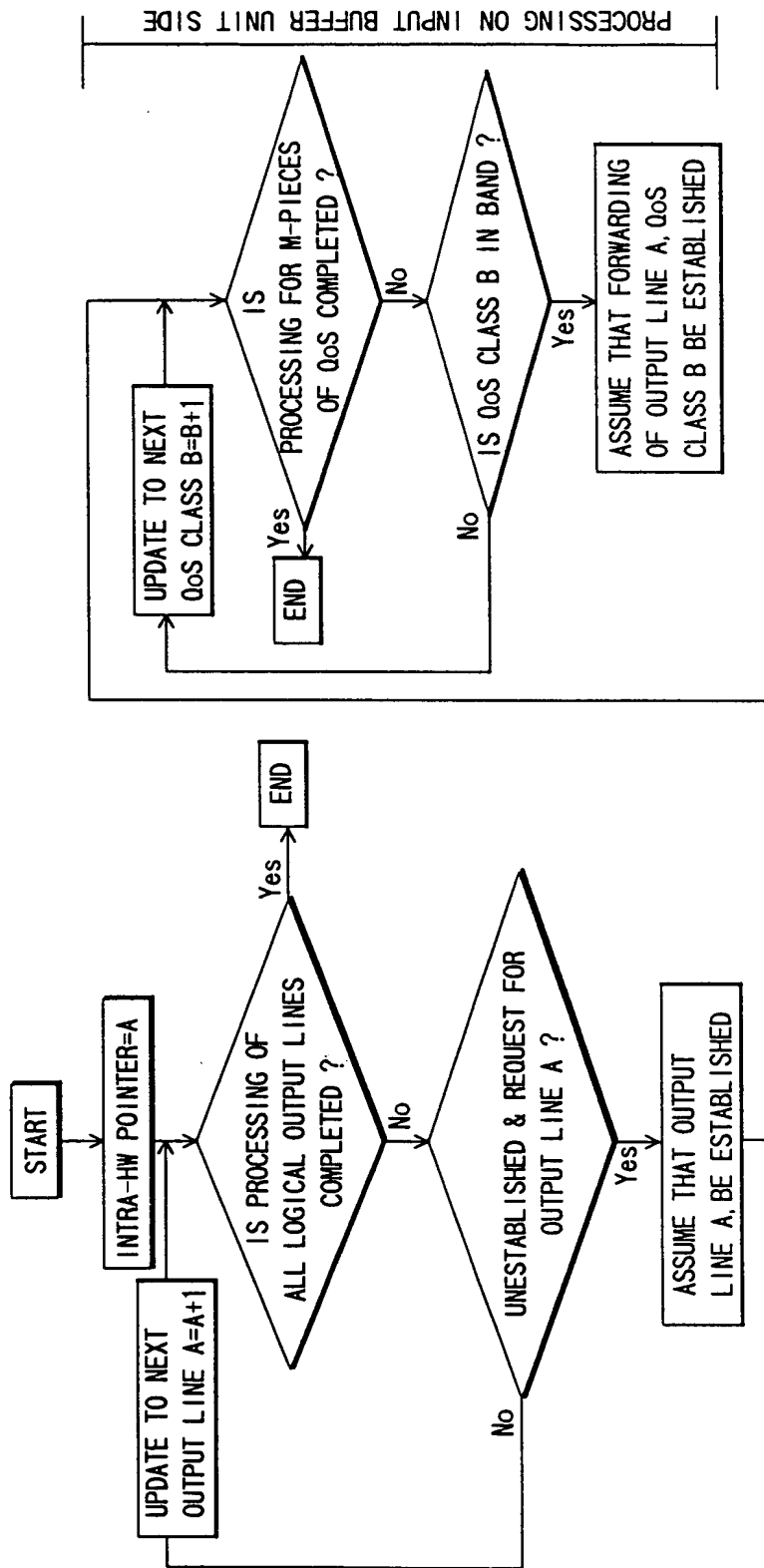


FIG.66

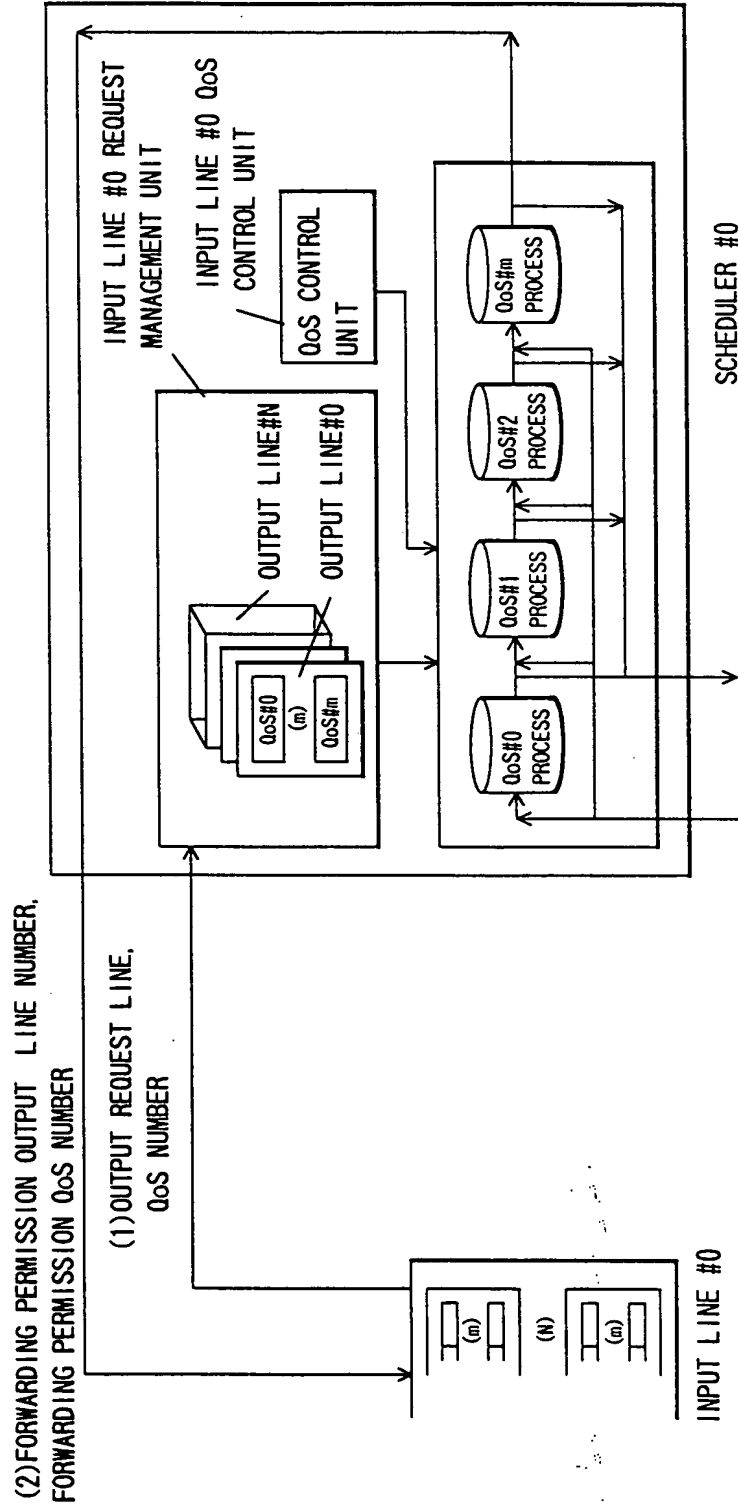


FIG.67

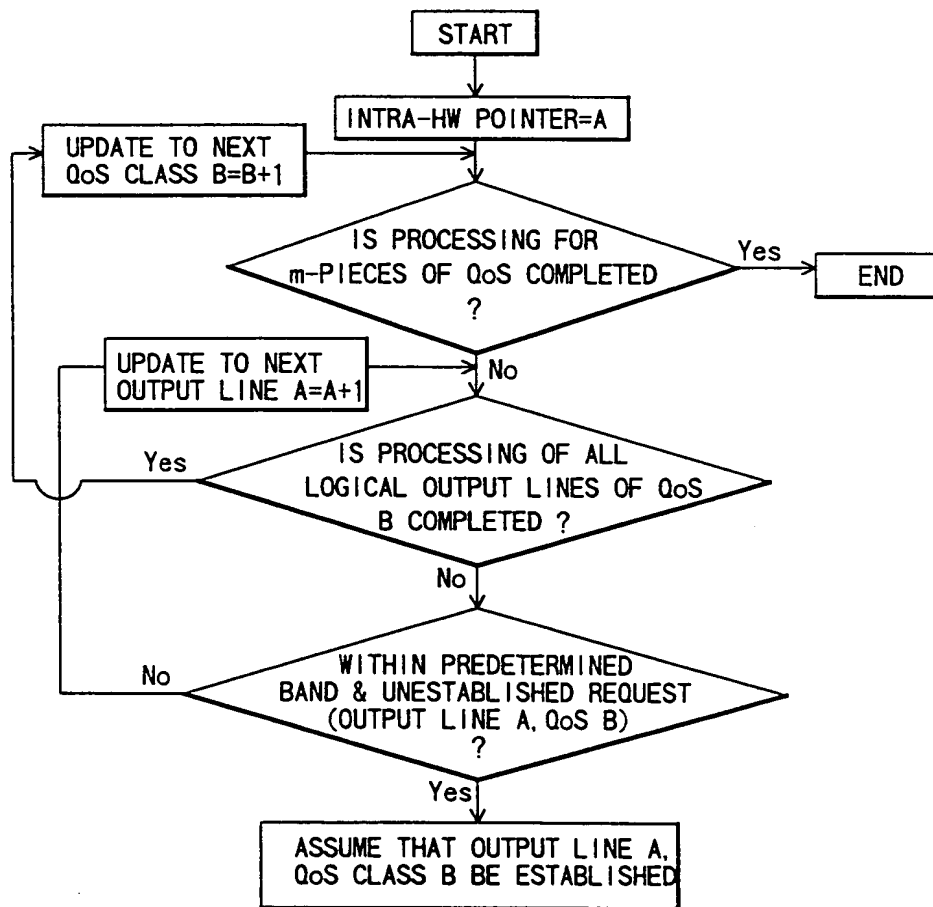


FIG.68

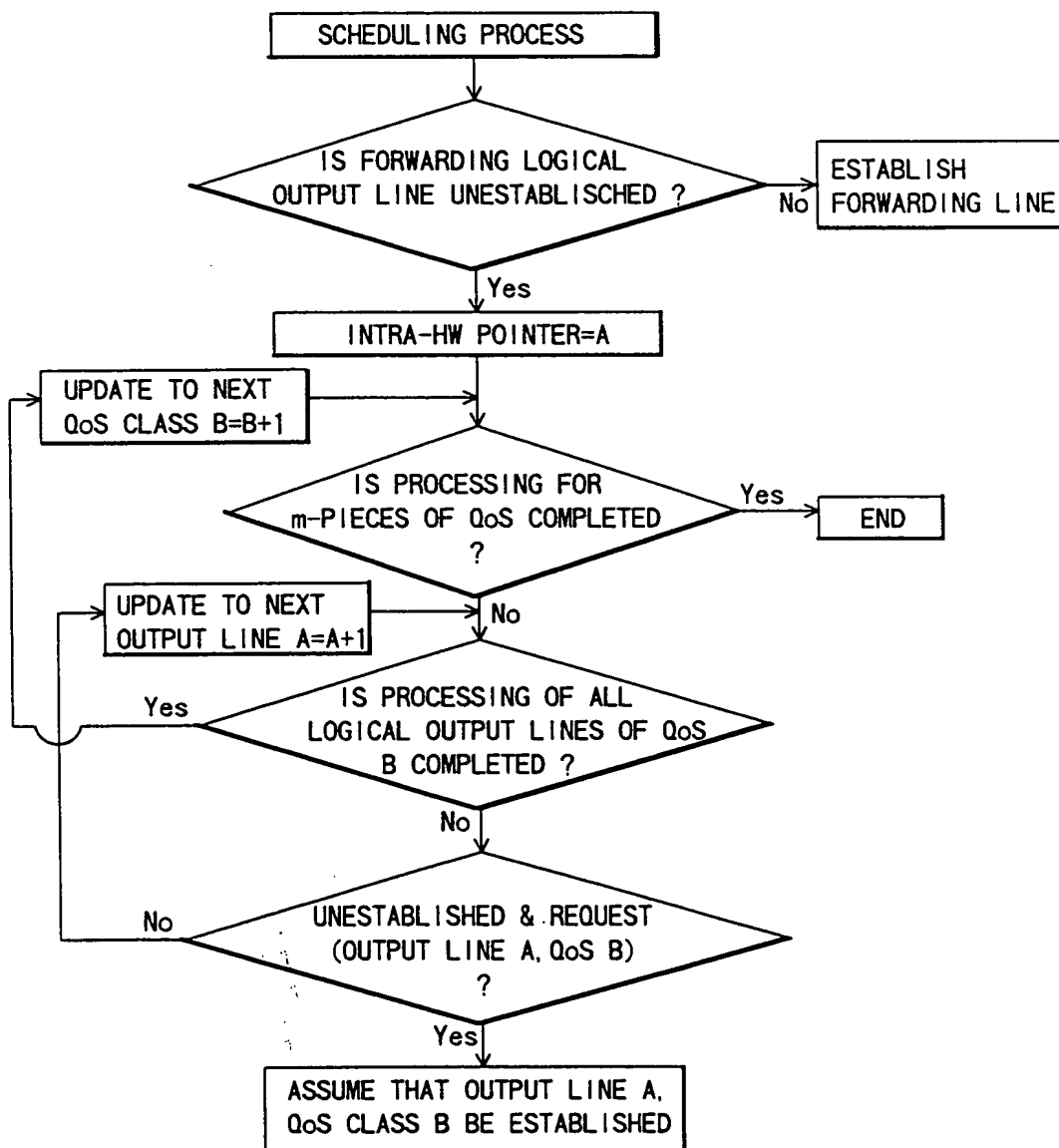


FIG.69

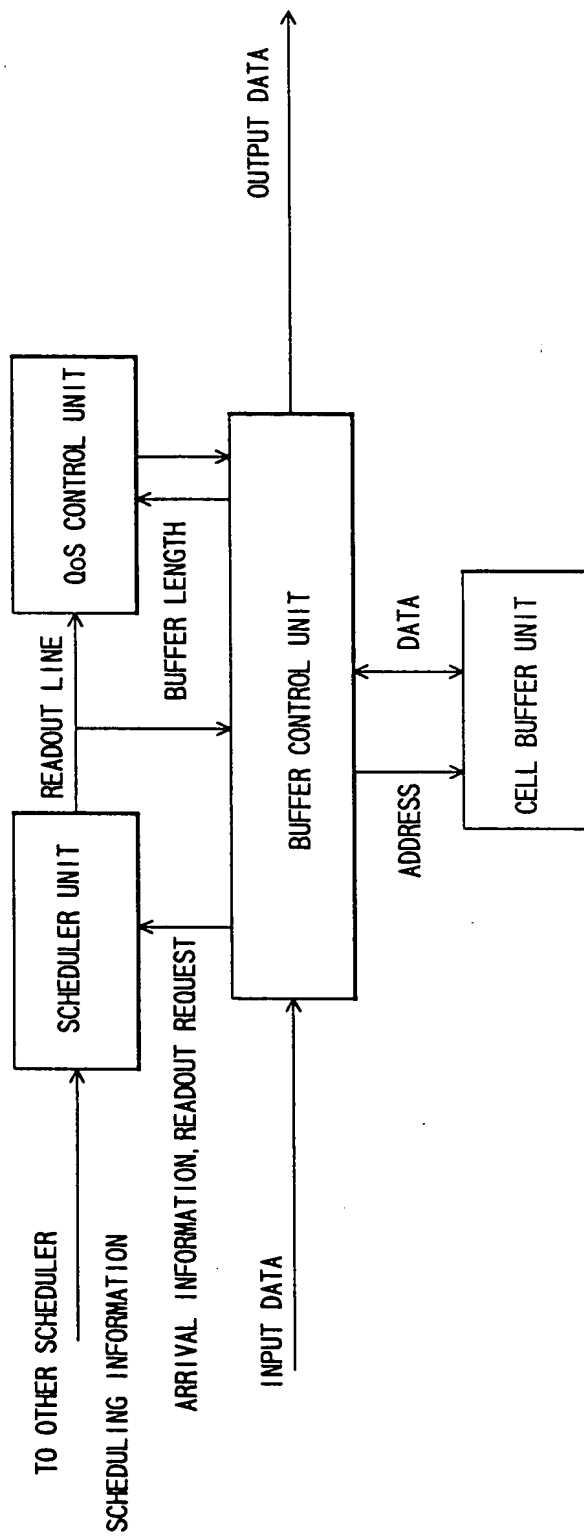
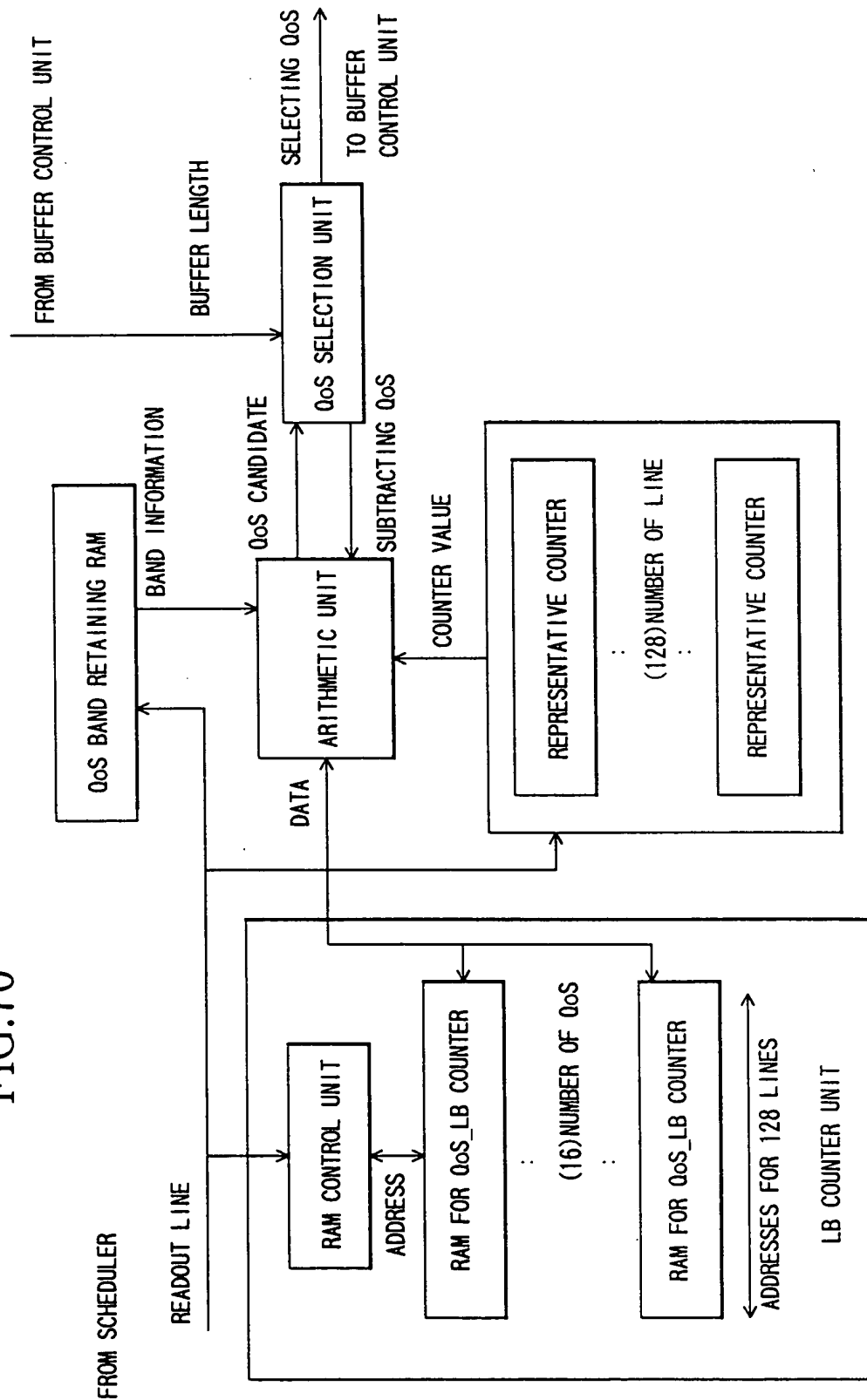


FIG.70



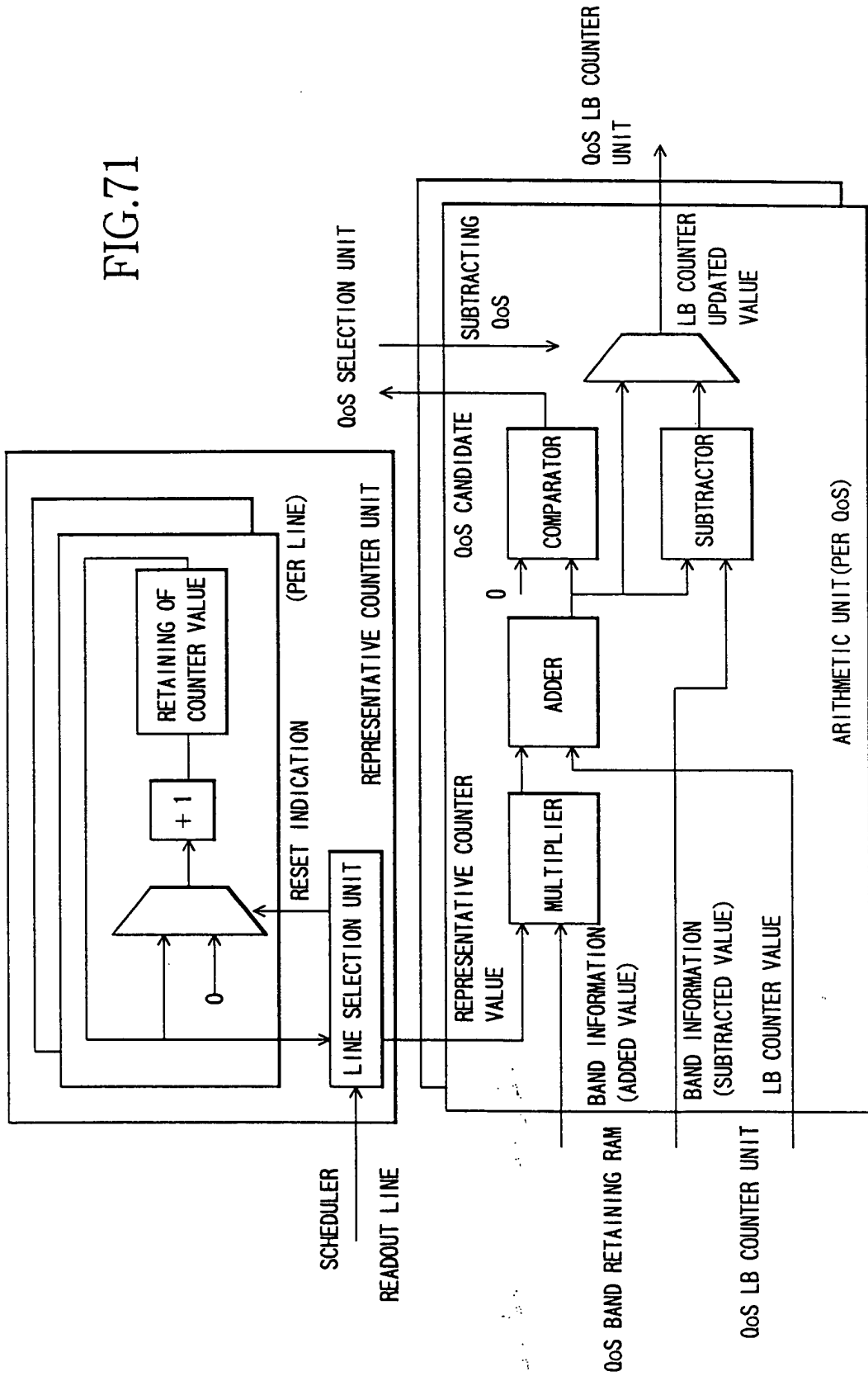


FIG. 71

FIG.72

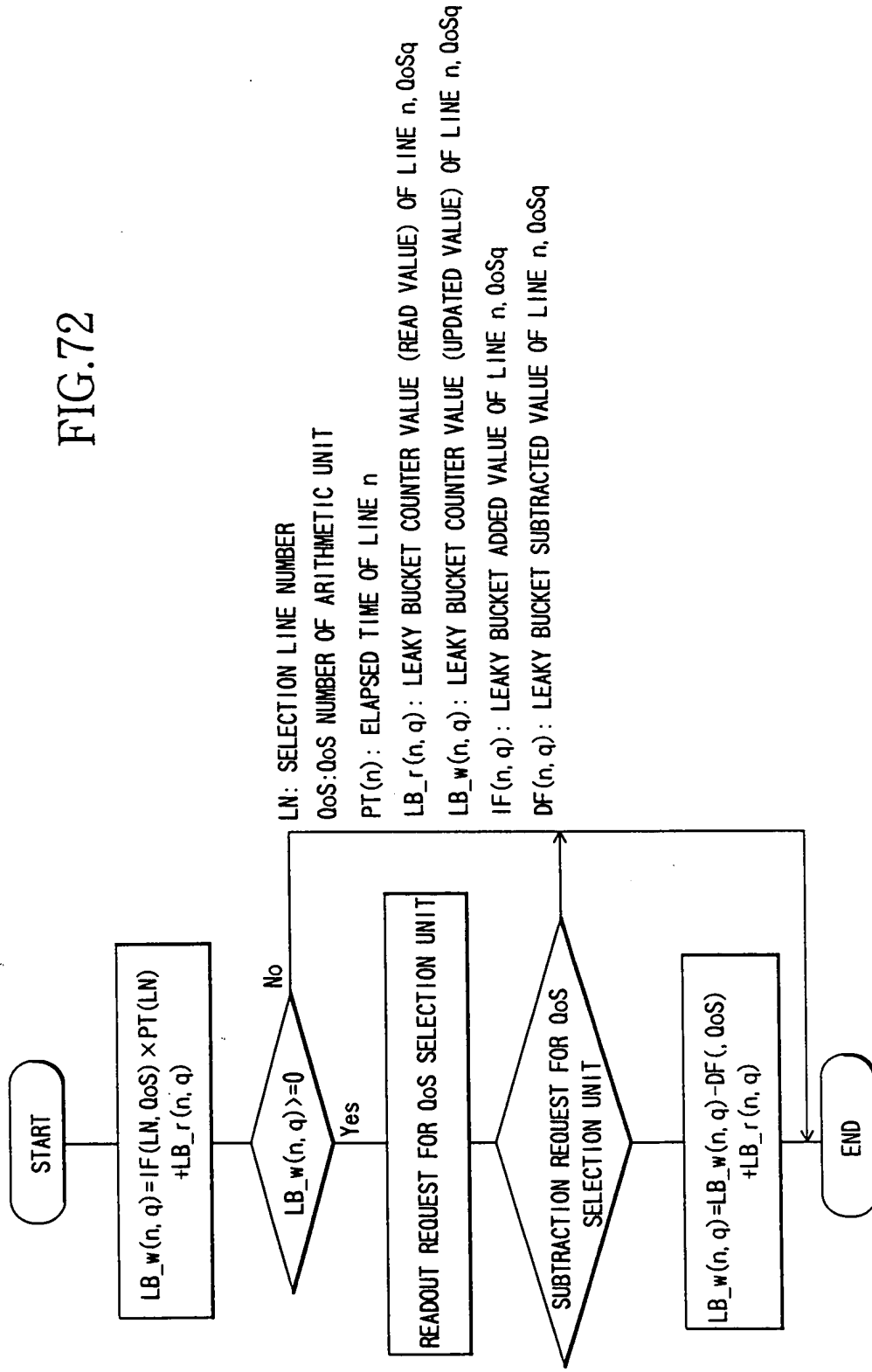


FIG. 73

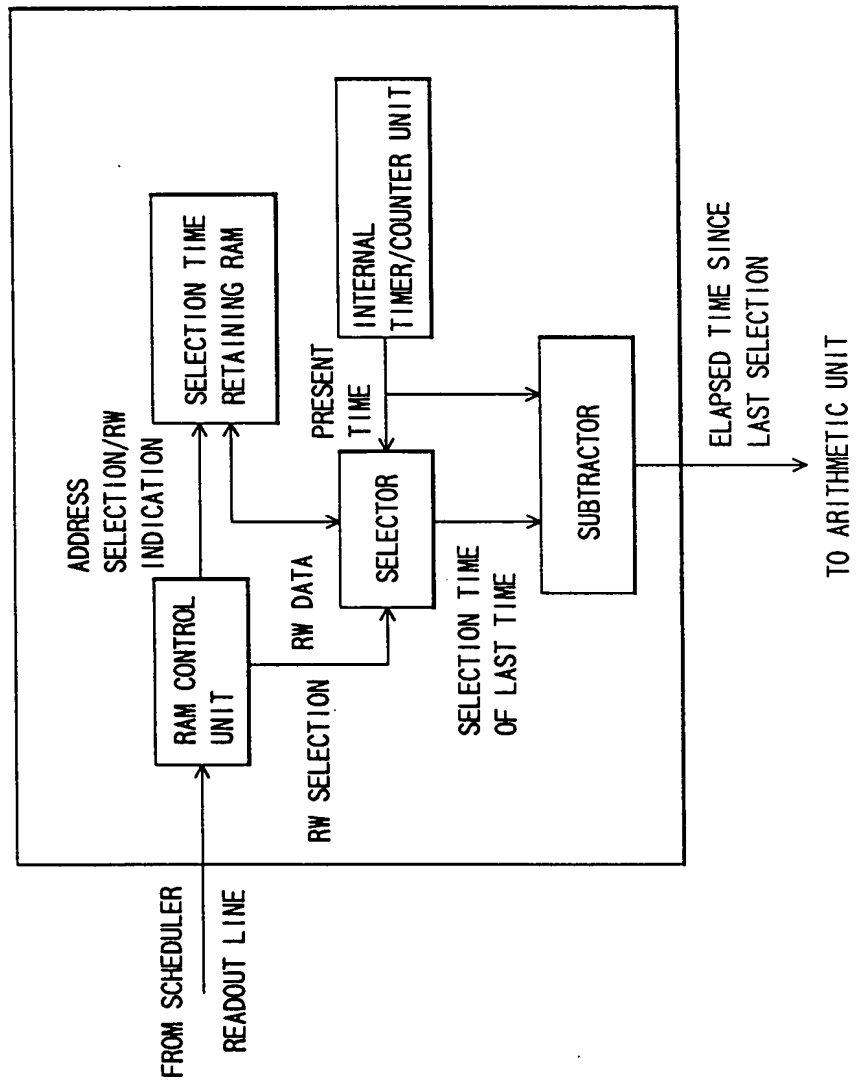


FIG. 74(a) LAST-TIME SELECTION TIME
RETAINING RAM BIT MAP (EXAMPLE)

SELECTION TIME VALID FLAG (1 BIT)

	SELECTION TIME (SAME NUMBER OF BITS AS INTERNAL TIMER)
--	--

FIG. 74(b) TIME REGION BASED VALID
TIME CHECKING METHOD

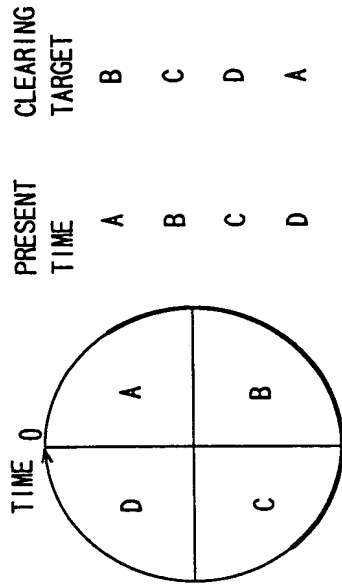
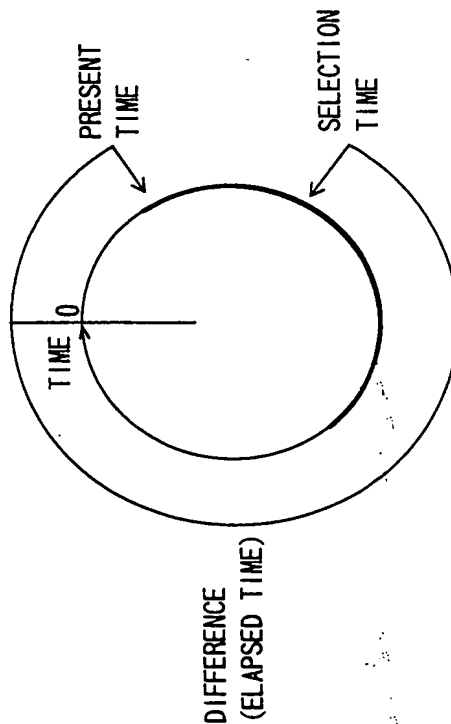
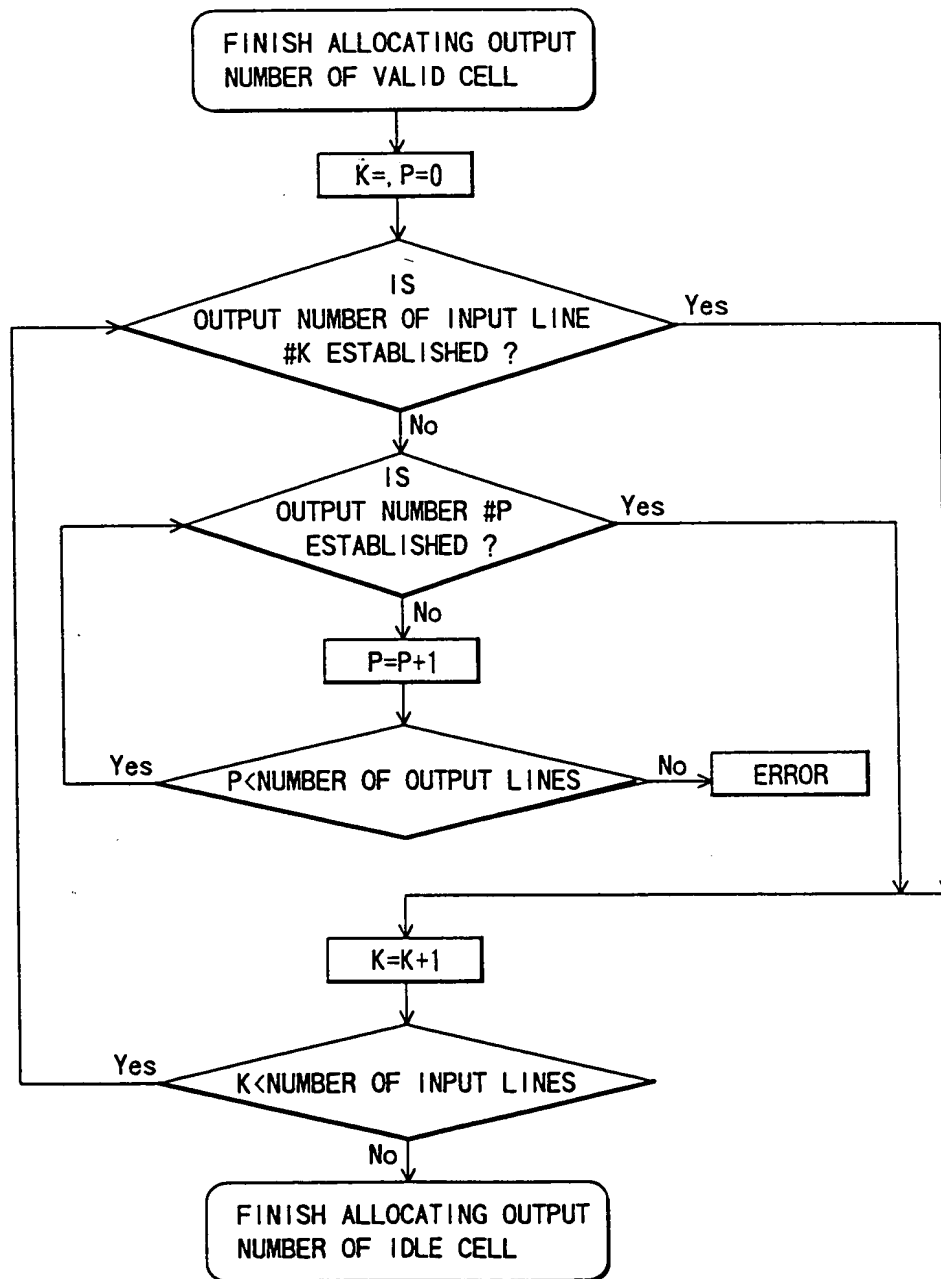


FIG. 74(c) THRESHOLD VALUE BASED
VALID TIME CHECKING METHOD



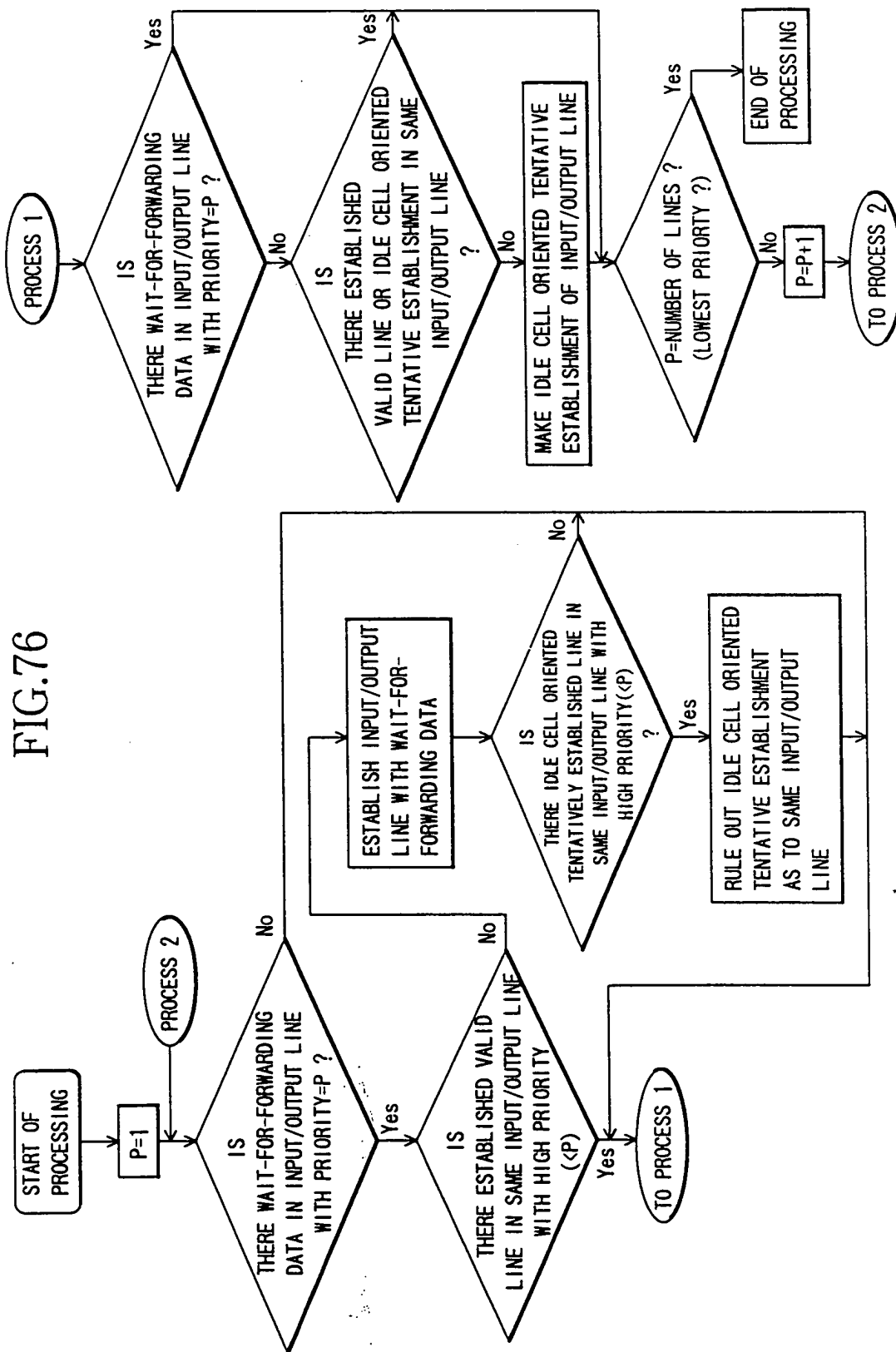
```
IF (VALID FLAG) = VALID
  IF (PRESENT TIME) > (SELECTION TIME)
    (DIFFERENCE) = (PRESENT TIME) - (SELECTION TIME)
  ELSE
    (DIFFERENCE) = (CYCLE) + (PRESENT TIME) - (SELECTION TIME)
  END IF
  IF (DIFFERENCE) > (THRESHOLD VALUE)
    (VALID FLAG) <= INVALID
```

FIG.75



0046088 12149 664727 36809460

FIG.76



09460898 121499

FIG.77

	POINTER=0→	POINTER=1→	POINTER=2→	POINTER=3
INPUT LINE #0	1	4	3	2
INPUT LINE #1	2	1	4	3
INPUT LINE #2	3	2	1	4
INPUT LINE #2	4	3	2	1

FIG.78

	POINTER=0→	POINTER=1→	POINTER=2→	POINTER=1
INPUT LINE #0	1	4	3	4
INPUT LINE #1	2	1	4	1
INPUT LINE #2	3	2	1	2
INPUT LINE #2	4	3	2	3

FIG.79

	1ST	2ND	3RD
INPUT LINE #0	OUTPUT LINE #0	OUTPUT LINE #2	OUTPUT LINE #1
INPUT LINE #1	OUTPUT LINE #2	OUTPUT LINE #1	OUTPUT LINE #0
INPUT LINE #2	OUTPUT LINE #1	OUTPUT LINE #0	OUTPUT LINE #2

FIG.80

	OUTPUT LINE #0	OUTPUT LINE #1	OUTPUT LINE #2
INPUT LINE #0	1	2	3
INPUT LINE #1	3	1	2
INPUT LINE #2	2	3	1